MINNOW2 BOARD Rev : A2

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REVISION HISTORY:

Rev	Date	Notes
A	2014/02/13	INITIAL RELEASE LISTED ADDITIONAL COMPATIBLE PART #'s on ON SPI ROM PAGE20 UPDATED DDR3L PART # on MEM1-MEM4 on PAGES 12-13 LISTED ADDITIONAL COMPATIBLE PART #'s ON DDR3L MEMORIES MEM1-MEM4 on PAGES 12-13
A1	2014/05/02	REWORK BOARD to REV_A1 PAGE 3 - ADD U39 INVERTER FOR HPD SIGNAL PAGE 6 - ADD R354 (0 OHM RES) to tie SD3_WP with SD3_CD#, DNI J6 HEADER. PAGE 7 - CHANGE R36,R98,R99,R103 = 0 OHMS UPDATE Y1, Y2 SYMBOLS UPDATE D5, D10 SYMBOLS PAGE 8 - CHANGE I2C5/I2C6 BUS NAMES PAGE 11 - TURN AROUND and DNI J2 HEADER, CHANGE MP1 HEATSINK PAGE 12 - UPDATE 0.047uF CAP SYMBOLS and MEM2/MEM3 SYMBOLS PAGE 13 - UPDATE 0.047uF CAP, 36R0 RES and MEM1/MEM4 SYMBOLS PAGE 14 - CHANGE R182 to 100K and PU to +V1P8S and change R180/R174/R173/R157/R156/R155 to 100K PAGE 15 - DNI R166, CHANGE R28-R30 = 10K PAGE 16 - DNI R115, UPDATE U32, L1/L2 SYMBOLS PAGE 17 - ADD PCIE TEST POINT VIAS (TP19-TP24), ADD +VSB to R18, +V1P8S TO R20, STUFF R21, CHANGE R6 PU FROM +V1P8A to +V1P8S, CHANGE R7 FROM 20K to 1K, CHANGE I2C6_SCL/SDA net names PAGE 18 - UPDATE Y3, J8 SYMBOL, ADD TP17-TP18 TEST POINTS PAGE 20 - UPDATE U3, D8 SYMBOLS, CHANGE R147 to 100K and PU TO +3VSB, UPDATE I2C5_SCL/SDA NET NAMES PAGE 21 - CHANGE BOARD MTG HOLE SYMBOLS to SUPPORT 6-32 screw. PAGE 22 - DNI R289, CHANGE R308 to 33 OHMS PAGE 23 - UPDATE CAP SYMBOLS (C36,C39,C61,C62) PS PH1 OPTIMIZE 1.) CHANGE C76,C77,C87 to LOWER ESR CAP 2.) CHANGE C40,C59 FROM 0.022uF to 0.047uF 3.) CHANGE R93 FROM 3.32KOHM to 2.6KOHM 4.) CHANGE R194 FROM 33KOHM to 80.6KOHM 5.) CHANGE R247 FROM 30KOHM to 80.6KOHM 6.) CHANGE R200 FROM 3.6KOHM to 3.32KOHM PAGE 25 - CHANGE C129 TO LOWER ESR CAP PAGE 27 - UPDATE GPIO SETTINGS DOCUMENTATION
A2	2014/10/22	REWORK BOARD to REV_A2 PAGE 23 - PS PH2 OPTIMIZE 1.) CHANGE R63 FROM 3.57KOHM to 2.67KOHM 2.) CHANGE R250 FROM 3.01KOHM to 2.61KOHM 3.) CHANGE R200 FROM 3.32KOHM to 2.43KOHM 4.) CHANGE R93 FROM 2.6KOHM to 2.21KOHM 5.) CHANGE C185 FROM 33pF to 68pF PAGE 7 - INSTALL R278 - FROM DNI to 1KOHM

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MINNOWBOARD2

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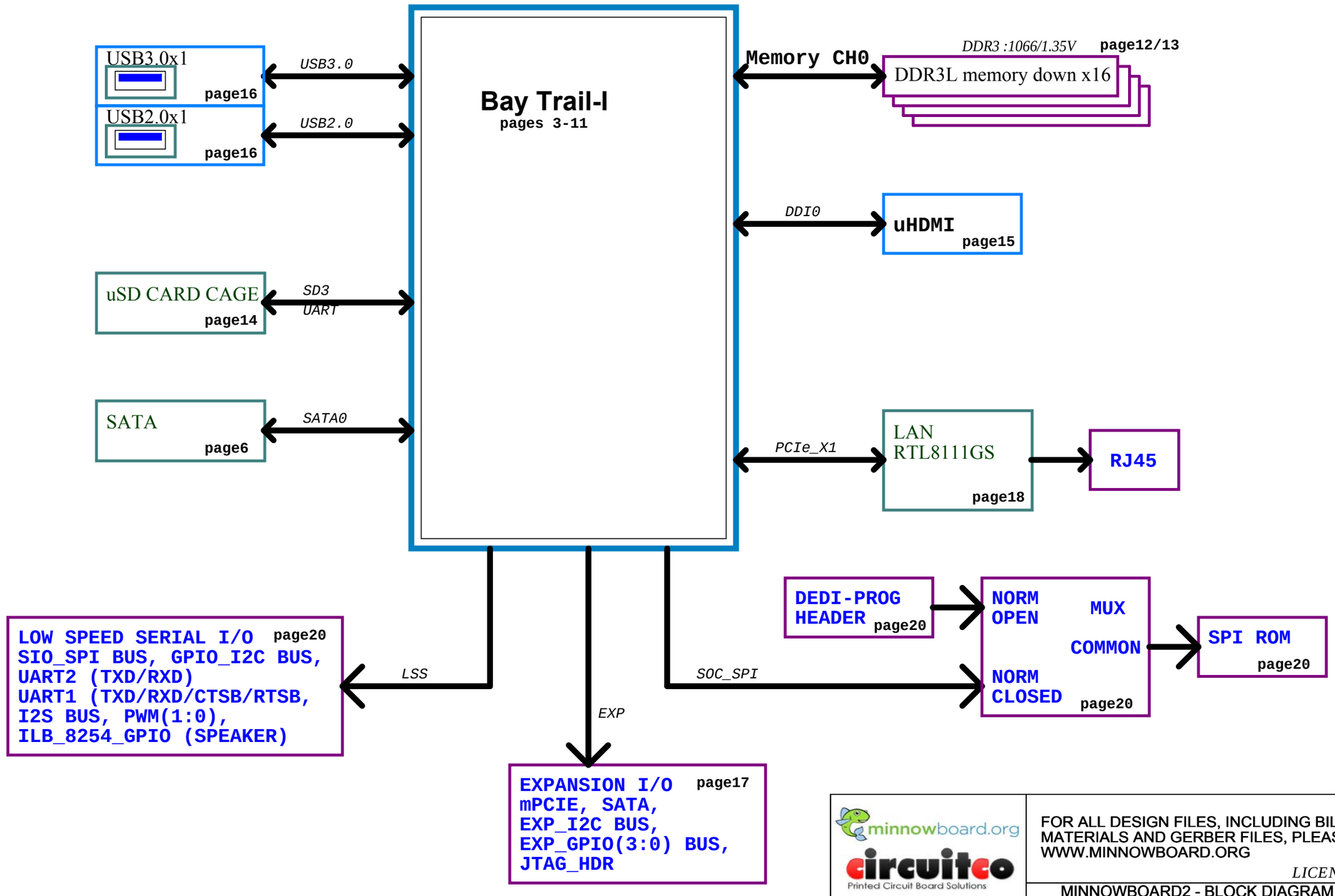

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MINNOWBOARD2 - BLOCK DIAGRAM

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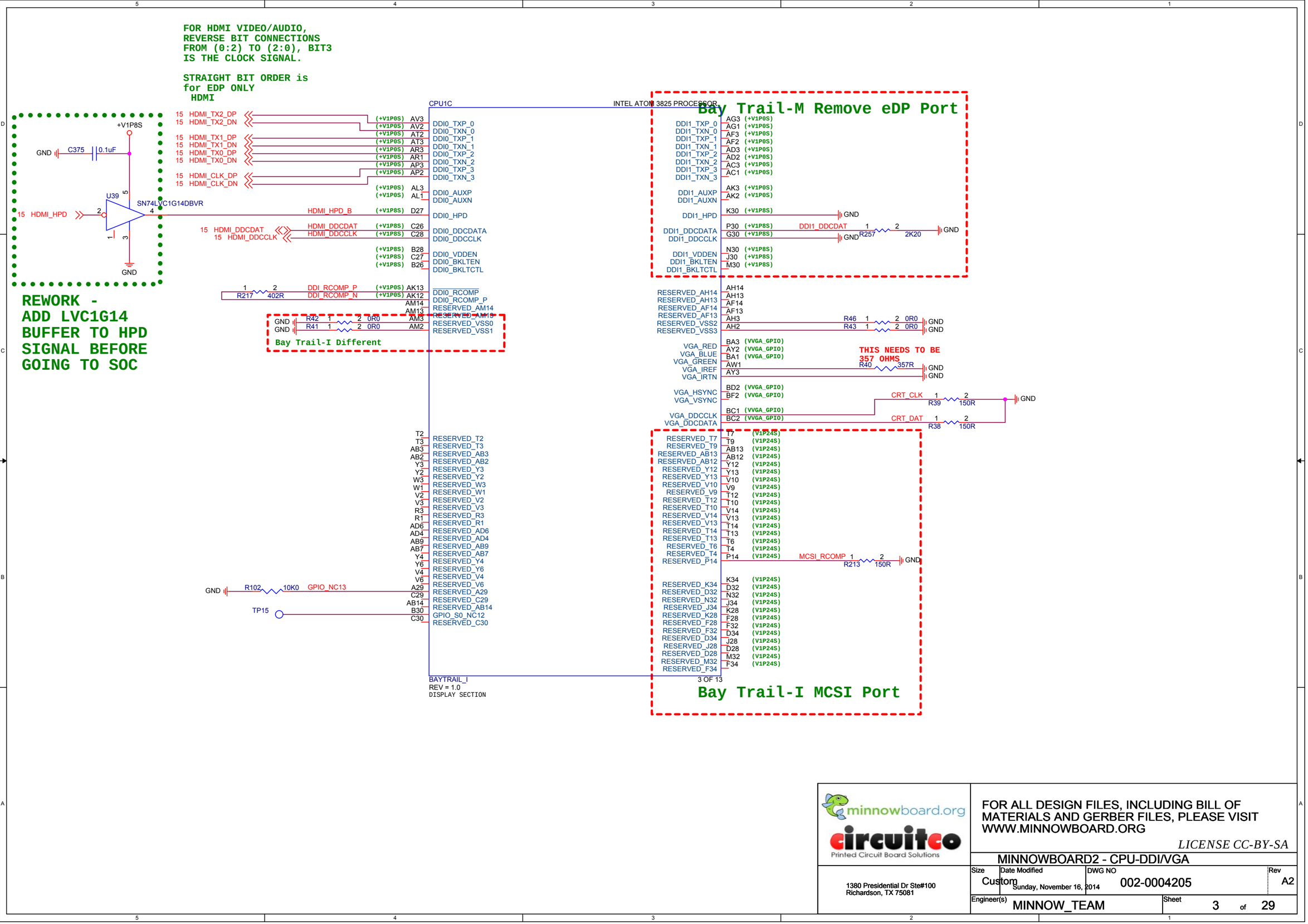

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MINNOWBOARD2 - CPU-DDI/VGA

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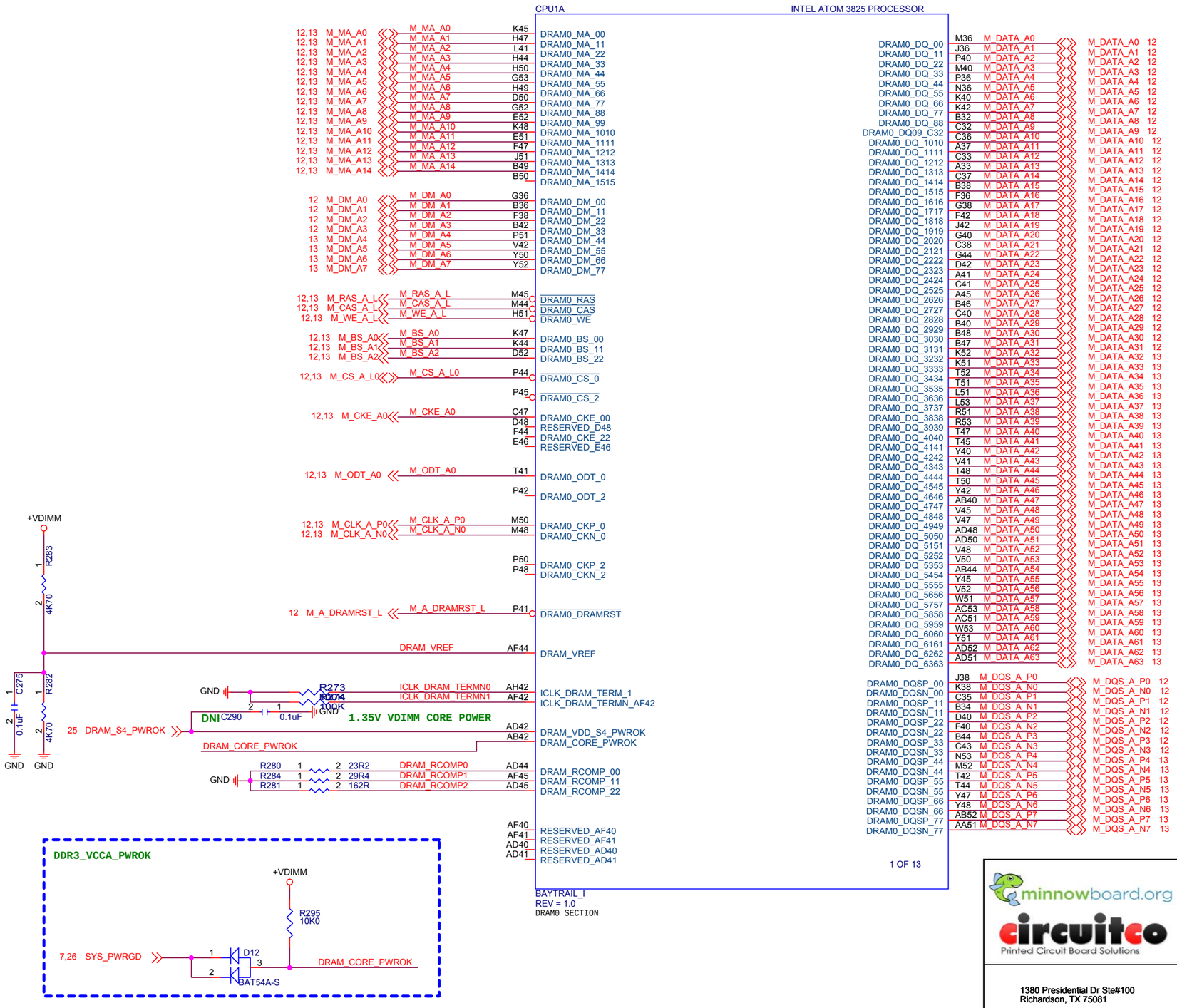

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MINNOWBOARD2 - CPU-DDR3-CHA

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CPU1B — INTEL ATOM 3825 PROCESSOR

AY45	DRAM1_MA_00
BB47	DRAM1_MA_11
AW41	DRAM1_MA_22
BB44	DRAM1_MA_33
BB50	DRAM1_MA_44
BC53	DRAM1_MA_55
BB49	DRAM1_MA_66
BF50	DRAM1_MA_77
BC52	DRAM1_MA_88
BE52	DRAM1_MA_99
AY48	DRAM1_MA_1010
BE51	DRAM1_MA_1111
BD47	DRAM1_MA_1212
BA51	DRAM1_MA_1313
BH49	DRAM1_MA_1414
BH50	DRAM1_MA_1515
BD38	DRAM1_DM_00
BH36	DRAM1_DM_11
BC36	DRAM1_DM_22
BH42	DRAM1_DM_33
AT51	DRAM1_DM_44
AM42	DRAM1_DM_55
AK50	DRAM1_DM_66
AK52	DRAM1_DM_77
AV45	DRAM1_RAS
AV44	DRAM1_CAS
BB51	DRAM1_WE
AY47	DRAM1_BS_00
AY44	DRAM1_BS_11
BF52	DRAM1_BS_22
AT44	DRAM1_CS_0
AT45	DRAM1_CS_2
BG47	DRAM1_CKE_00
BE46	RESERVED_BE46
BD44	DRAM1_CKE_22
BF48	RESERVED_BF48
AP41	DRAM1_ODT_0
AT42	DRAM1_ODT_2
AV50	DRAM1_CKP_0
AV48	DRAM1_CKN_0
AT50	DRAM1_CKP_2
AT48	DRAM1_CKN_2
AT41	DRAM1_DRAMRST

BG38	DRAM1_DQ_00
BC40	DRAM1_DQ_11
BA42	DRAM1_DQ_22
BD42	DRAM1_DQ_33
BC38	DRAM1_DQ_44
BD36	DRAM1_DQ_55
BF42	DRAM1_DQ_66
BC44	DRAM1_DQ_77
BH32	DRAM1_DQ_88
BG32	DRAM1_DQ_99
BG36	DRAM1_DQ_1010
BJ37	DRAM1_DQ_1111
BG33	DRAM1_DQ_1212
BJ33	DRAM1_DQ_1313
BG37	DRAM1_DQ_1414
BH38	DRAM1_DQ_1515
AU36	DRAM1_DQ_1616
AT36	DRAM1_DQ_1717
AV40	DRAM1_DQ_1818
AT40	DRAM1_DQ_1919
BA36	DRAM1_DQ_2020
AV36	DRAM1_DQ_2121
AY42	DRAM1_DQ_2222
AY40	DRAM1_DQ_2323
BJ41	DRAM1_DQ_2424
BG41	DRAM1_DQ_2525
BJ45	DRAM1_DQ_2626
BH46	DRAM1_DQ_2727
BG40	DRAM1_DQ_2828
BH40	DRAM1_DQ_2929
BH48	DRAM1_DQ_3030
BH47	DRAM1_DQ_3131
AY52	DRAM1_DQ_3232
AY51	DRAM1_DQ_3333
AP52	DRAM1_DQ_3434
AP51	DRAM1_DQ_3535
AW51	DRAM1_DQ_3636
AW53	DRAM1_DQ_3737
AR51	DRAM1_DQ_3838
AR53	DRAM1_DQ_3939
AP47	DRAM1_DQ_4040
AP45	DRAM1_DQ_4141
AK40	DRAM1_DQ_4242
AM41	DRAM1_DQ_4343
AP48	DRAM1_DQ_4444
AP50	DRAM1_DQ_4545
AK42	DRAM1_DQ_4646
AH40	DRAM1_DQ_4747
AM45	DRAM1_DQ_4848
AM47	DRAM1_DQ_4949
AF48	DRAM1_DQ_5050
AF50	DRAM1_DQ_5151
AM48	DRAM1_DQ_5252
AM50	DRAM1_DQ_5353
AH44	DRAM1_DQ_5454
AK45	DRAM1_DQ_5555
AM52	DRAM1_DQ_5656
AL51	DRAM1_DQ_5757
AG53	DRAM1_DQ_5858
AG51	DRAM1_DQ_5959
AL53	DRAM1_DQ_6060
AK51	DRAM1_DQ_6161
AF52	DRAM1_DQ_6262
AF51	DRAM1_DQ_6363
BF40	DRAM1_DQSP_00
BD40	DRAM1_DQSN_00
BG35	DRAM1_DQSP_11
BH34	DRAM1_DQSN_11
BA38	DRAM1_DQSP_22
AY38	DRAM1_DQSN_22
BH44	DRAM1_DQSP_33
BG43	DRAM1_DQSN_33
AU53	DRAM1_DQSP_44
AV52	DRAM1_DQSN_44
AP42	DRAM1_DQSP_55
AP44	DRAM1_DQSN_55
AK47	DRAM1_DQSP_66
AK48	DRAM1_DQSN_66
AH52	DRAM1_DQSP_77
AJ51	DRAM1_DQSN_77

BAYTRAIL_I — 2 OF 13

REV = 1.0

DRAM1 SECTION

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MINNOWBOARD2 - CPU-DDR3-CHB

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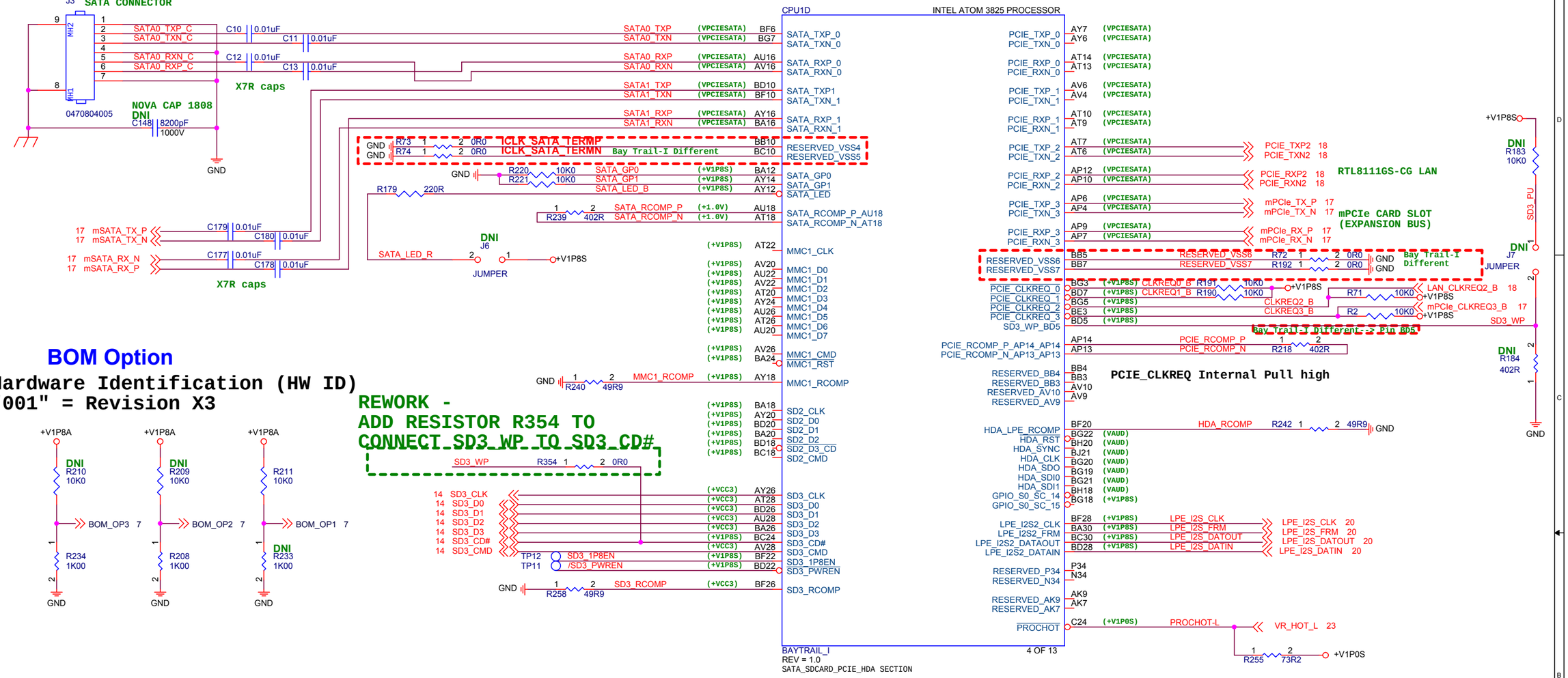
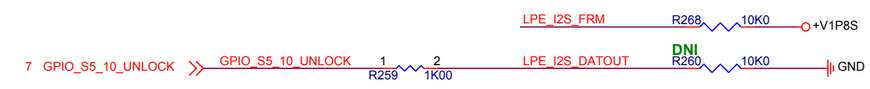


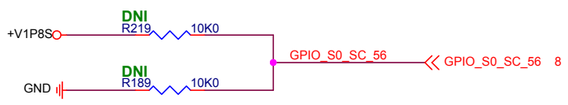
BOM Option

Hardware Identification (HW ID)
"001" = Revision X3



HW STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC



Top Swap(A16 Override)

H	Top address bit is unchanged
L	Top address bit is inverted

Strap Pin	Function
GPIO_S0_SC63 (LPE_I2S_FRM)	BIOS Boot Selection 0=LPC *1=SPI
GPIO_S0_SC65 (LPE_I2S_DATOUT)	Security Flash Descriptors 0=Override *1=Normal Operation

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MINNOWBOARD2 - CPU-PE/HDA/SD/eMMC/Strap

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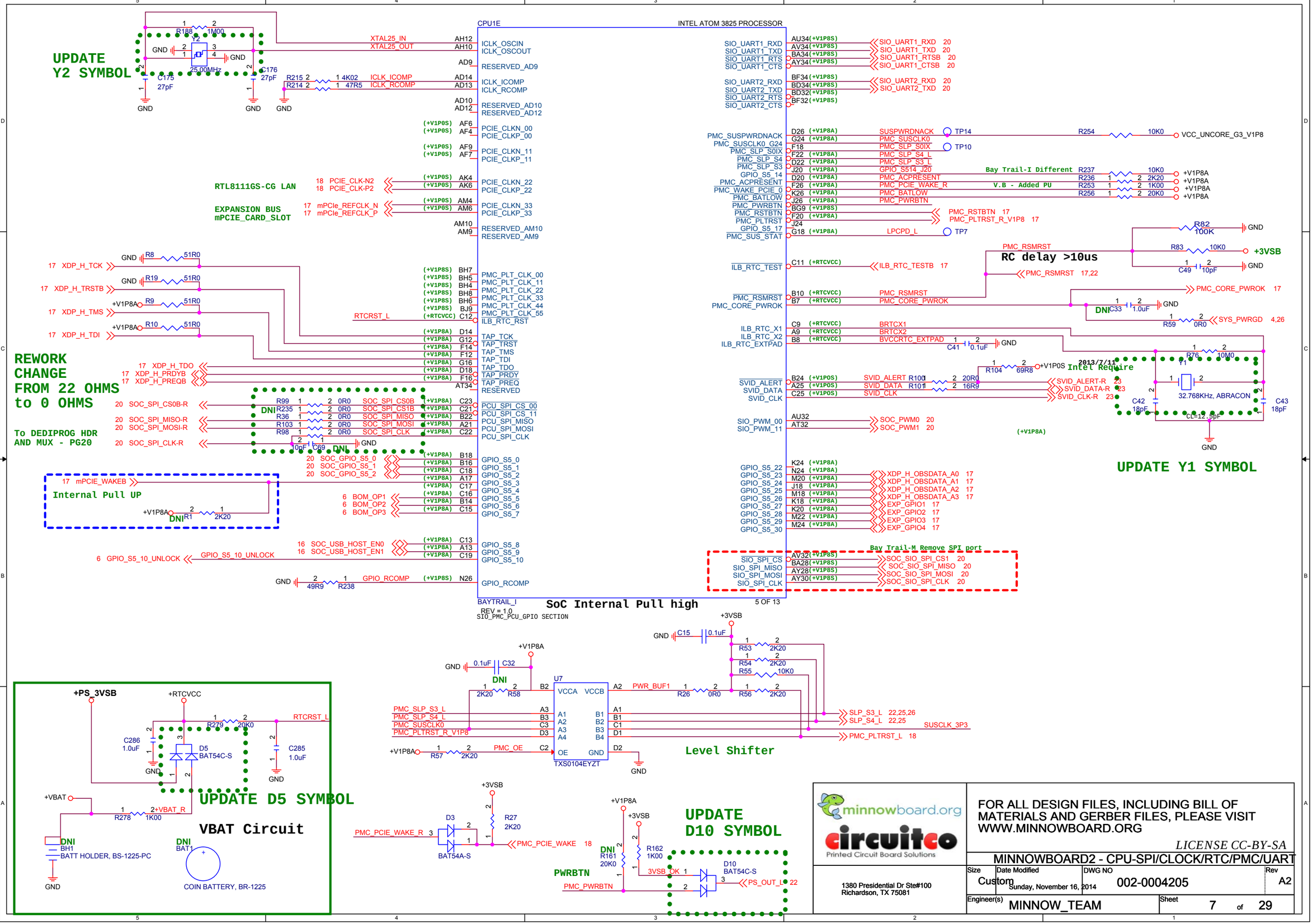
UPDATE Y2 SYMBOL
Y2
25.00MHz
R188 1M00
C175 27pF
C176 27pF
GND
XTAL25_IN
XTAL25_OUT
R215 4K02
R214 47R5
ICLK_ICOMP
ICLK_RCOMP
CPU1E
INTEL ATOM 3825 PROCESSOR
ICLK_OSCIN
ICLK_OSCOUT
RESERVED_AD9
ICLK_ICOMP
ICLK_RCOMP
RESERVED_AD10
RESERVED_AD12
PCIE_CLKN_00
PCIE_CLKP_00
PCIE_CLKN_11
PCIE_CLKP_11
RTL8111GS-CG LAN
18 PCIE_CLK-N2
18 PCIE_CLK-P2
PCIE_CLKN_22
PCIE_CLKP_22
EXPANSION BUS
mPCIE_CARD_SLOT
17 mPCIe_REFCLK_N
17 mPCIe_REFCLK_P
PCIE_CLKN_33
PCIE_CLKP_33
RESERVED_AM10
RESERVED_AM9
17 XDP_H_TCK
17 XDP_H_TRSTB
17 XDP_H_TMS
17 XDP_H_TDI
R8 51R0
R19 51R0
R9 51R0
R10 51R0
+V1P8A
PMC_PLT_CLK_00
PMC_PLT_CLK_11
PMC_PLT_CLK_22
PMC_PLT_CLK_33
PMC_PLT_CLK_44
PMC_PLT_CLK_55
RTCRST_L
ILB_RTC_RST
TAP_TCK
TAP_TRST
TAP_TMS
TAP_TDI
TAP_TDO
TAP_PRDY
TAP_PREQ
RESERVED
REWORK CHANGE FROM 22 OHMS to 0 OHMS
17 XDP_H_TDO
17 XDP_H_PRDYB
17 XDP_H_PREQB
20 SOC_SPI_CS0B-R
20 SOC_SPI_MISO-R
20 SOC_SPI_MOSI-R
20 SOC_SPI_CLK-R
R99 0R0
R235 0R0
R36 0R0
R103 0R0
R98 0R0
SOC_SPI_CS0B
SOC_SPI_CS1B
SOC_SPI_MISO
SOC_SPI_MOSI
SOC_SPI_CLK
DNI
C69 10pF
To DEDIPROG HDR AND MUX - PG20
PCU_SPI_CS_00
PCU_SPI_CS_11
PCU_SPI_MISO
PCU_SPI_MOSI
PCU_SPI_CLK
20 SOC_GPIO_S5_0
20 SOC_GPIO_S5_1
20 SOC_GPIO_S5_2
17 mPCIE_WAKEB
Internal Pull UP
R1 2K20
6 BOM_OP1
6 BOM_OP2
6 BOM_OP3
16 SOC_USB_HOST_EN0
16 SOC_USB_HOST_EN1
6 GPIO_S5_10_UNLOCK
GPIO_S5_10_UNLOCK
GPIO_RCOMP
R238 49R9
GPIO_S5_0
GPIO_S5_1
GPIO_S5_2
GPIO_S5_3
GPIO_S5_4
GPIO_S5_5
GPIO_S5_6
GPIO_S5_7
GPIO_S5_8
GPIO_S5_9
GPIO_S5_10
BAYTRAIL_I
REV = 1.0
SIO_PMC_PCU_GPIO SECTION
SoC Internal Pull high
5 OF 13
SIO_UART1_RXD
SIO_UART1_TXD
SIO_UART1_RTS
SIO_UART1_CTS
SIO_UART2_RXD
SIO_UART2_TXD
SIO_UART2_RTS
SIO_UART2_CTS
SIO_UART1_RXD 20
SIO_UART1_TXD 20
SIO_UART1_RTSB 20
SIO_UART1_CTSB 20
SIO_UART2_RXD 20
SIO_UART2_TXD 20
PMC_SUSPWRDNACK
PMC_SUSCLK0_G24
PMC_SLP_S0IX
PMC_SLP_S4
PMC_SLP_S3
GPIO_S5_14
PMC_ACPRESENT
PMC_WAKE_PCIE_0
PMC_BATLOW
PMC_PWRBTN
PMC_RSTBTN
PMC_PLTRST
GPIO_S5_17
PMC_SUS_STAT
SUSPWRDNACK
PMC_SUSCLK0
PMC_SLP_S0IX
PMC_SLP_S4_L
PMC_SLP_S3_L
GPIO_S514_J20
PMC_ACPRESENT
PMC_PCIE_WAKE_R
PMC_BATLOW
PMC_PWRBTN
LPCPD_L
TP14
TP10
TP7
Bay Trail-I Different
V.B - Added PU
R254 10K0
R237 10K0
R236 2K20
R253 1K00
R256 20K0
VCC_UNCORE_G3_V1P8
+V1P8A
PMC_RSTBTN 17
PMC_PLTRST_R_V1P8 17
R82 100K
PMC_RSMRST
RC delay >10us
R83 10K0
+3VSB
C49 10pF
ILB_RTC_TEST
ILB_RTC_TESTB 17
PMC_RSMRST 17,22
PMC_CORE_PWROK 17
PMC_CORE_PWROK
C33 1.0uF
R59 0R0
SYS_PWRGD 4,26
ILB_RTC_X1
ILB_RTC_X2
ILB_RTC_EXTPAD
BRTCX1
BRTCX2
BVCCRTC_EXTPAD
C41 0.1uF
R104 69R8
+V1P0S
2013/7/11
Intel Require
R76 10M0
Y1
32.768KHz, ABRACON
CL=12.5pF
C42 18pF
C43 18pF
SVID_ALERT
SVID_DATA
SVID_CLK
R100 20R0
R101 16R9
SVID_ALERT-R 23
SVID_DATA-R 23
SVID_CLK-R 23
SIO_PWM_00
SIO_PWM_11
SOC_PWM0 20
SOC_PWM1 20
(+V1P8A)
UPDATE Y1 SYMBOL
XDP_H_OBSDATA_A0 17
XDP_H_OBSDATA_A1 17
XDP_H_OBSDATA_A2 17
XDP_H_OBSDATA_A3 17
EXP_GPIO1 17
EXP_GPIO2 17
EXP_GPIO3 17
EXP_GPIO4 17
Bay Trail-M Remove SPI port
SIO_SPI_CS
SIO_SPI_MISO
SIO_SPI_MOSI
SIO_SPI_CLK
SOC_SIO_SPI_CS1 20
SOC_SIO_SPI_MISO 20
SOC_SIO_SPI_MOSI 20
SOC_SIO_SPI_CLK 20
+PS_3VSB
+RTCVCC
R279 20K0
C286 1.0uF
D5 BAT54C-S
C285 1.0uF
UPDATE D5 SYMBOL
+VBAT
R278 1K00
+VBAT_R
VBAT Circuit
BH1
BATT HOLDER, BS-1225-PC
BAT1
COIN BATTERY, BR-1225
+3VSB
C15 0.1uF
R53 2K20
R54 2K20
R55 10K0
+V1P8A
C32 0.1uF
R58 2K20
U7
VCCA
VCCB
PWR_BUF1
R26 0R0
R56 2K20
PMC_SLP_S3_L
PMC_SLP_S4_L
PMC_SUSCLK0
PMC_PLTRST_R_V1P8
PMC_OE
R57 2K20
TXS0104EYZT
SLP_S3_L 22,25,26
SLP_S4_L 22,25
SUSCLK_3P3
PMC_PLTRST_L 18
Level Shifter
D3 BAT54A-S
R27 2K20
PMC_PCIE_WAKE_R
PMC_PCIE_WAKE 18
UPDATE D10 SYMBOL
R161 20K0
R162 1K00
3VSB_OK
D10 BAT54C-S
PWRBTN
PMC_PWRBTN
PS_OUT_L 22
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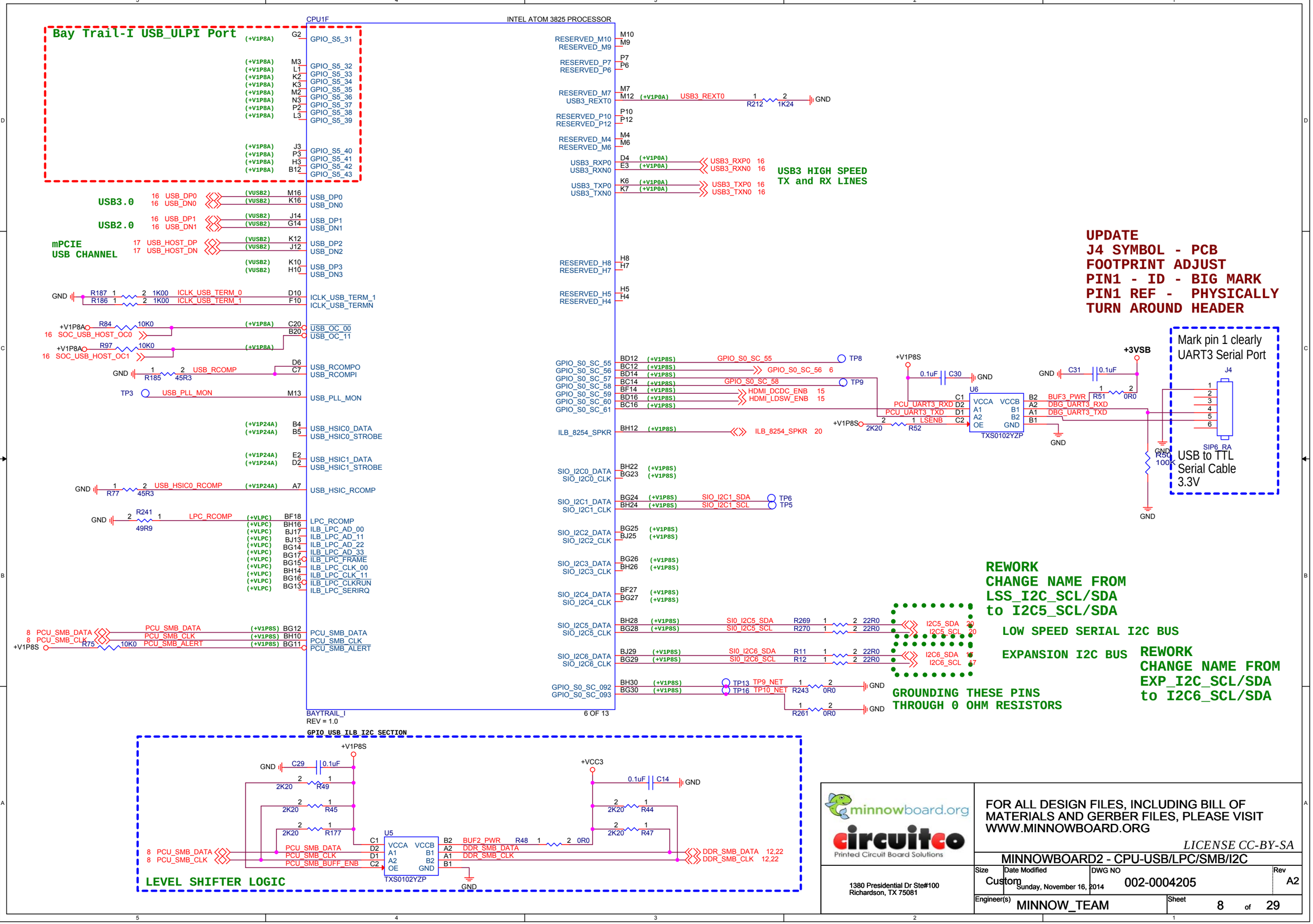
CPU1F
INTEL ATOM 3825 PROCESSOR
Bay Trail-I USB_ULPI Port
USB3.0
USB2.0
mPCIE
USB CHANNEL
USB3 HIGH SPEED
TX and RX LINES
UPDATE
J4 SYMBOL - PCB
FOOTPRINT ADJUST
PIN1 - ID - BIG MARK
PIN1 REF - PHYSICALLY
TURN AROUND HEADER
Mark pin 1 clearly
UART3 Serial Port
USB to TTL
Serial Cable
3.3V
REWORK
CHANGE NAME FROM
LSS_I2C_SCL/SDA
to I2C5_SCL/SDA
LOW SPEED SERIAL I2C BUS
EXPANSION I2C BUS
REWORK
CHANGE NAME FROM
EXP_I2C_SCL/SDA
to I2C6_SCL/SDA
GROUNDING THESE PINS
THROUGH 0 OHM RESISTORS
BAYTRAIL_I
REV = 1.0
6 OF 13
GPIO USB ILB I2C SECTION
LEVEL SHIFTER LOGIC
TXS0102YZP
SIP6_RA
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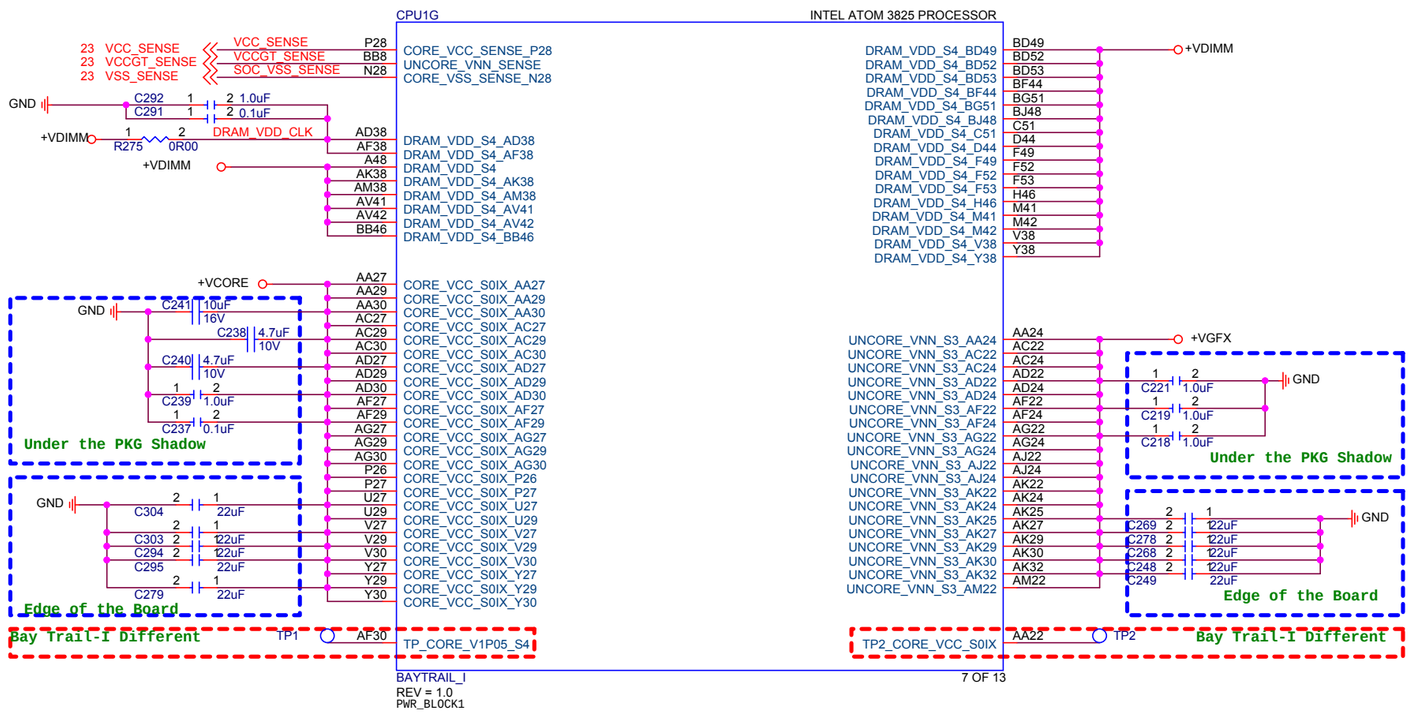

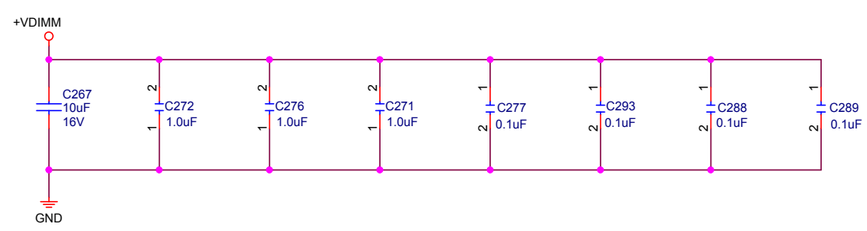

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MINNOWBOARD2 - CPU-PWR1/TPM/LPC

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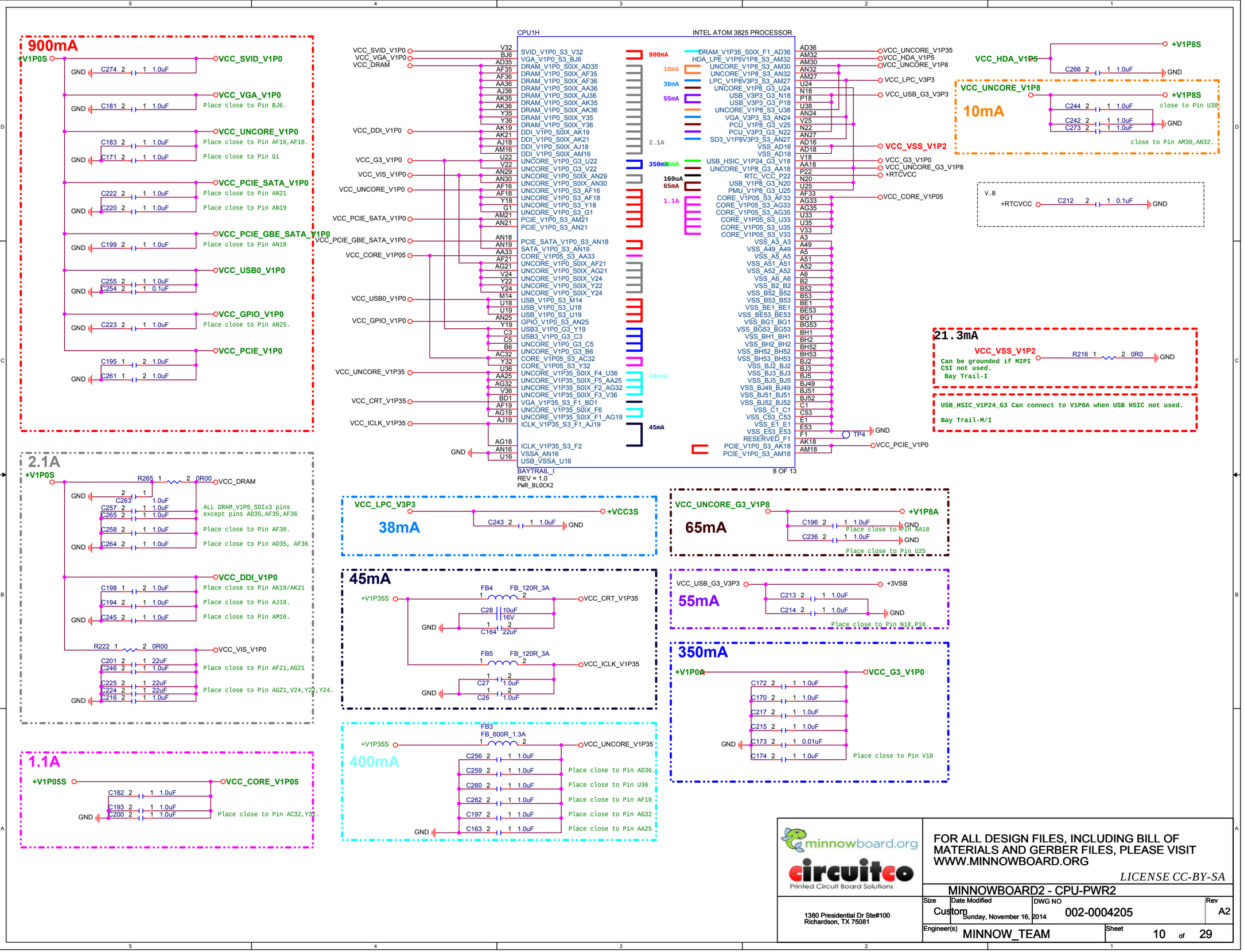
900mA
+V1P0S
VCC_SVID_V1P0
VCC_VGA_V1P0
Place close to Pin BJ6.
VCC_UNCORE_V1P0
Place close to Pin AF16,AF18.
Place close to Pin G1
VCC_PCIE_SATA_V1P0
Place close to Pin AN21
Place close to Pin AN19
VCC_PCIE_GBE_SATA_V1P0
Place close to Pin AN18
VCC_USB0_V1P0
VCC_GPIO_V1P0
Place close to Pin AN25.
VCC_PCIE_V1P0
2.1A
+V1P0S
VCC_DRAM
ALL DRAM_V1P0_SOIx3 pins except pins AD35,AF35,AF36
Place close to Pin AF36.
Place close to Pin AD35, AF36
VCC_DDI_V1P0
Place close to Pin AK19/AK21
Place close to Pin AJ18.
Place close to Pin AM16.
VCC_VIS_V1P0
Place close to Pin AF21,AG21
Place close to Pin AG21,V24,Y22,Y24.
1.1A
+V1P05S
VCC_CORE_V1P05
Place close to Pin AC32,Y32.
CPU1H
INTEL ATOM 3825 PROCESSOR
BAYTRAIL_I
REV = 1.0
PWR_BLOCK2
8 OF 13
900mA
10mA
38mA
55mA
2.1A
350mA
160uA
65mA
1.1A
400mA
45mA
VCC_SVID_V1P0
VCC_VGA_V1P0
VCC_DRAM
VCC_DDI_V1P0
VCC_G3_V1P0
VCC_VIS_V1P0
VCC_UNCORE_V1P0
VCC_PCIE_SATA_V1P0
VCC_PCIE_GBE_SATA_V1P0
VCC_CORE_V1P05
VCC_USB0_V1P0
VCC_GPIO_V1P0
VCC_UNCORE_V1P35
VCC_CRT_V1P35
VCC_ICLK_V1P35
GND
VCC_UNCORE_V1P35
VCC_HDA_V1P5
VCC_LPC_V3P3
VCC_USB_G3_V3P3
VCC_VSS_V1P2
VCC_G3_V1P0
VCC_UNCORE_G3_V1P8
+RTCVCC
VCC_CORE_V1P05
TP4
VCC_PCIE_V1P0
+V1P8S
VCC_HDA_V1P5
C266 2 1 1.0uF GND
VCC_UNCORE_V1P8
10mA
+V1P8S
close to Pin U38.
C244 2 1 1.0uF
C242 2 1 1.0uF
C273 2 1 1.0uF
GND
close to Pin AM30,AN32.
V.B
+RTCVCC
C212 2 1 0.1uF GND
21.3mA
VCC_VSS_V1P2
Can be grounded if MIPI CSI not used.
Bay Trail-I
R216 1 2 0R0 GND
USB_HSIC_V1P24_G3 Can connect to V1P0A when USB HSIC not used.
Bay Trail-M/I
VCC_LPC_V3P3
38mA
+VCC3S
C243 2 1 1.0uF GND
VCC_UNCORE_G3_V1P8
65mA
+V1P8A
C196 2 1 1.0uF
Place close to Pin AA18
C236 2 1 1.0uF
Place close to Pin U25
45mA
+V1P35S
FB4 FB_120R_3A
VCC_CRT_V1P35
C28 10uF 16V
C164 22uF
FB5 FB_120R_3A
VCC_ICLK_V1P35
C27 1.0uF
C26 1.0uF
VCC_USB_G3_V3P3
+3VSB
55mA
C213 2 1 1.0uF
C214 2 1 1.0uF
Place close to Pin N18,P18.
350mA
+V1P0A
VCC_G3_V1P0
C172 2 1 1.0uF
C170 2 1 1.0uF
C217 2 1 1.0uF
C215 2 1 1.0uF
C173 2 1 0.01uF
C174 2 1 1.0uF
Place close to Pin V18
400mA
FB3 FB_600R_1.3A
+V1P35S
VCC_UNCORE_V1P35
C256 2 1 1.0uF
C259 2 1 1.0uF
C260 2 1 1.0uF
C262 2 1 1.0uF
C197 2 1 1.0uF
C163 2 1 1.0uF
Place close to Pin AD36.
Place close to Pin U36
Place close to Pin AF19
Place close to Pin AG32
Place close to Pin AA25
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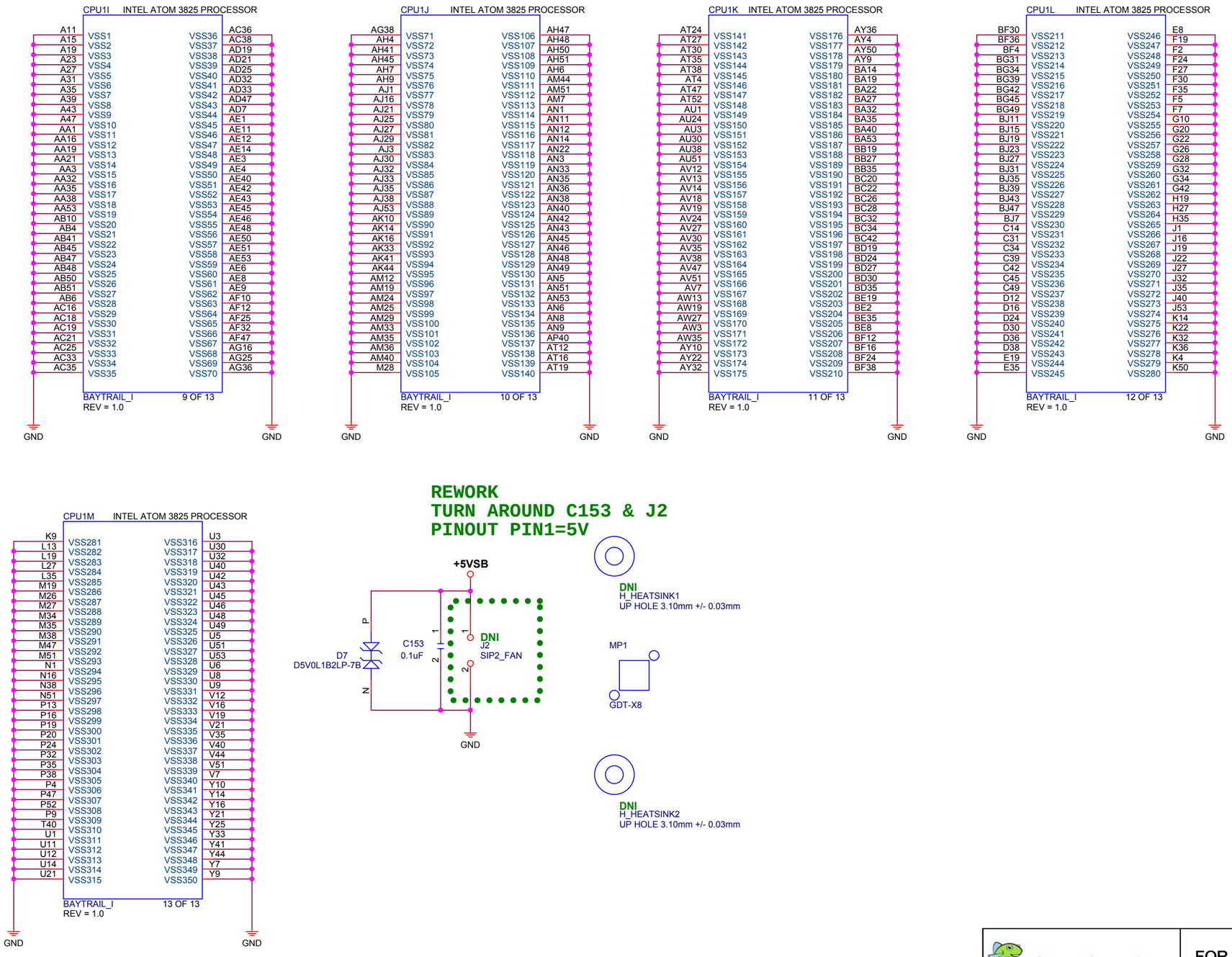
MINNOWBOARD2 - CPU-PWR2
Size Custom
Date Modified Sunday, November 16, 2014
DWG NO 002-0004205
Rev A2
Engineer(s) MINNOW_TEAM
Sheet 10 of 29



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MINNOWBOARD2 - CPU-GND

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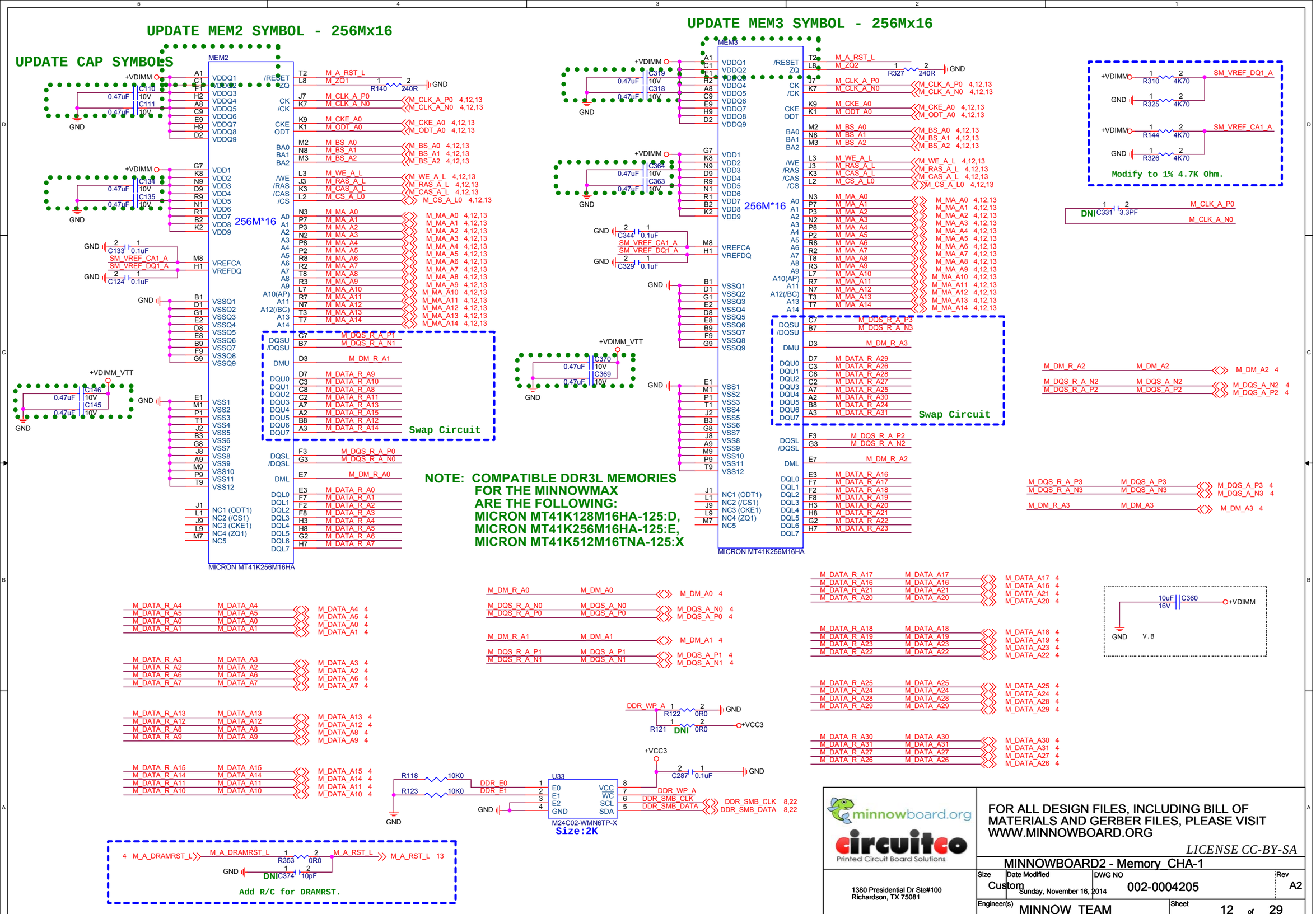
UPDATE MEM2 SYMBOL - 256Mx16
UPDATE MEM3 SYMBOL - 256Mx16
UPDATE CAP SYMBOLS
MEM2
MICRON MT41K256M16HA
256M*16
MEM3
MICRON MT41K256M16HA
256M*16
Swap Circuit
Swap Circuit
NOTE: COMPATIBLE DDR3L MEMORIES
FOR THE MINNOWMAX
ARE THE FOLLOWING:
MICRON MT41K128M16HA-125:D,
MICRON MT41K256M16HA-125:E,
MICRON MT41K512M16TNA-125:X
Modify to 1% 4.7K Ohm.
DNI
Add R/C for DRAMRST.
U33
M24C02-WMN6TP-X
Size:2K
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MINNOWBOARD2 - Memory_CHA-1
Size Custom
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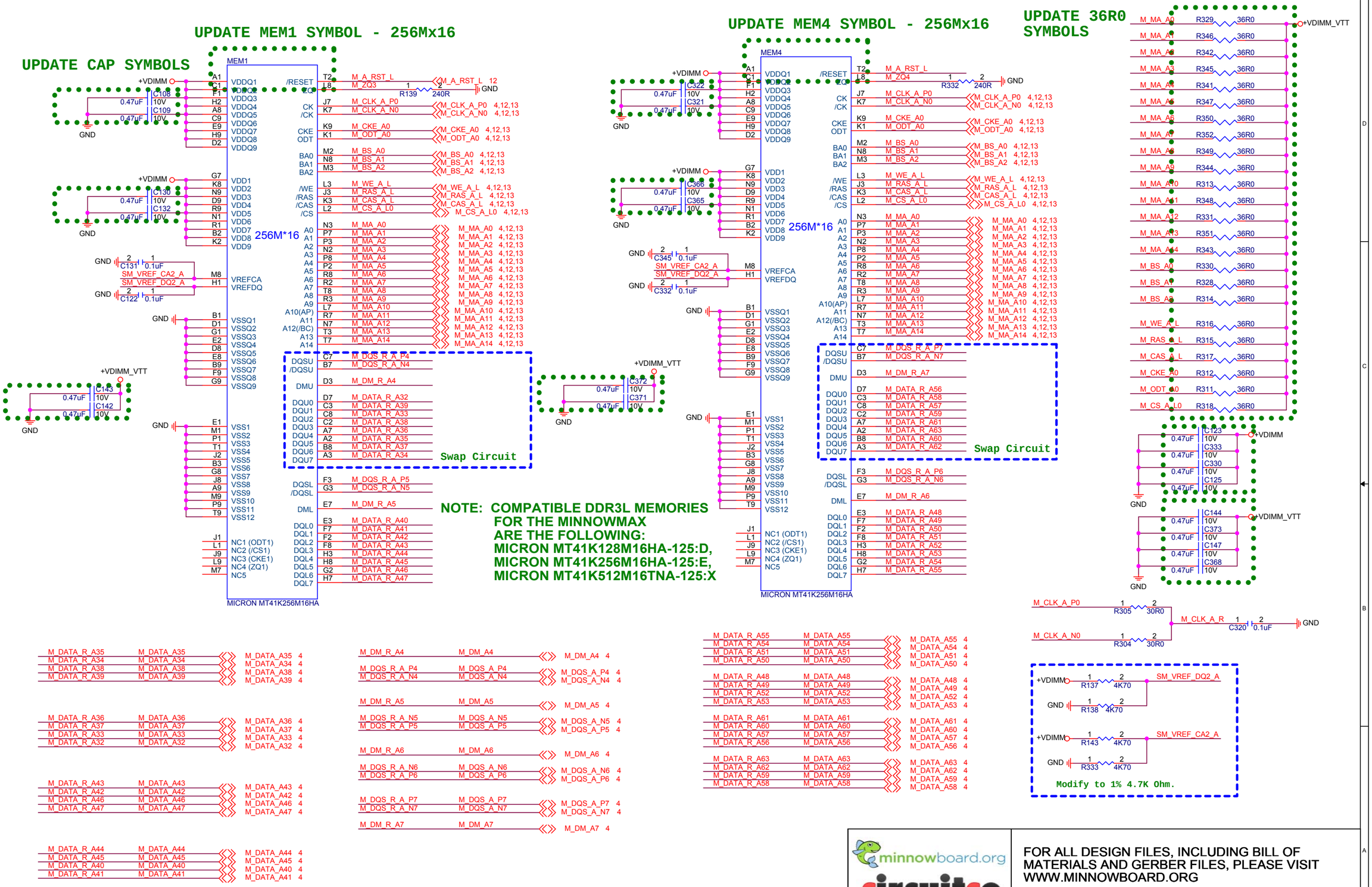

MINNOWBOARD2 - Memory_CHA-2

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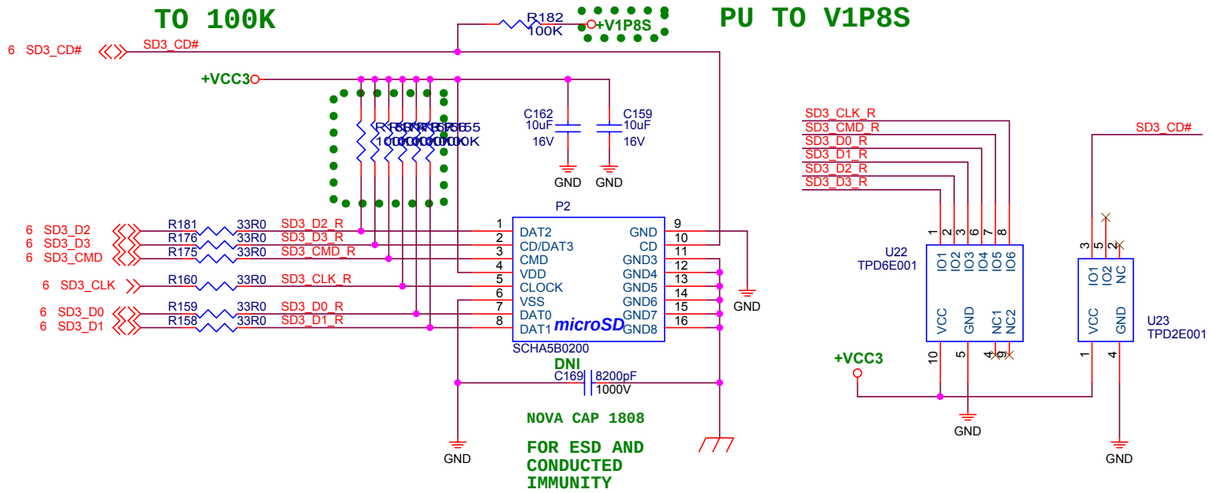
REWORK -
R180,R174,R173,
R157,R156,R155
CHANGE
FROM 10K
TO 100K

REWORK -
R182
CHANGE
to 100K &
PU TO V1P8S



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MINNOWBOARD2 - uSD CARD CAGE

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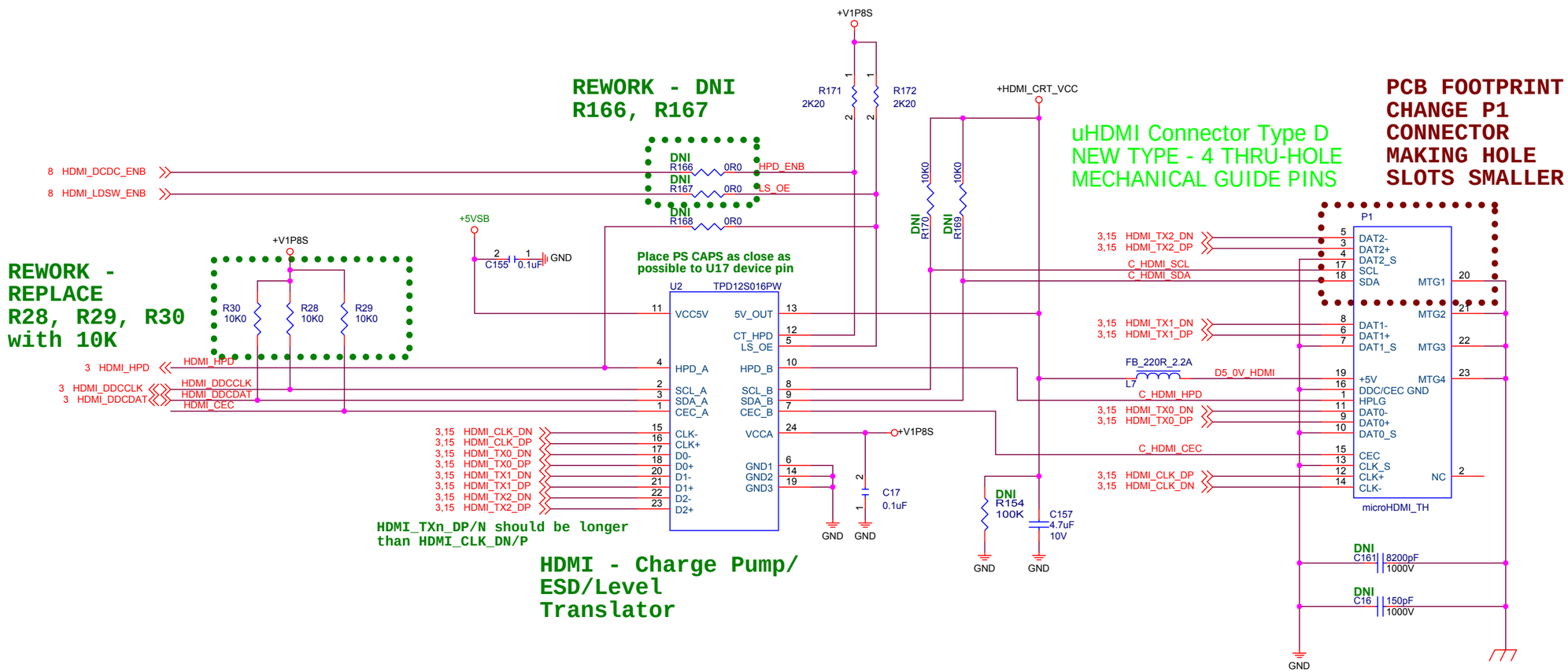

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MINNOWBOARD2 - uHDMI

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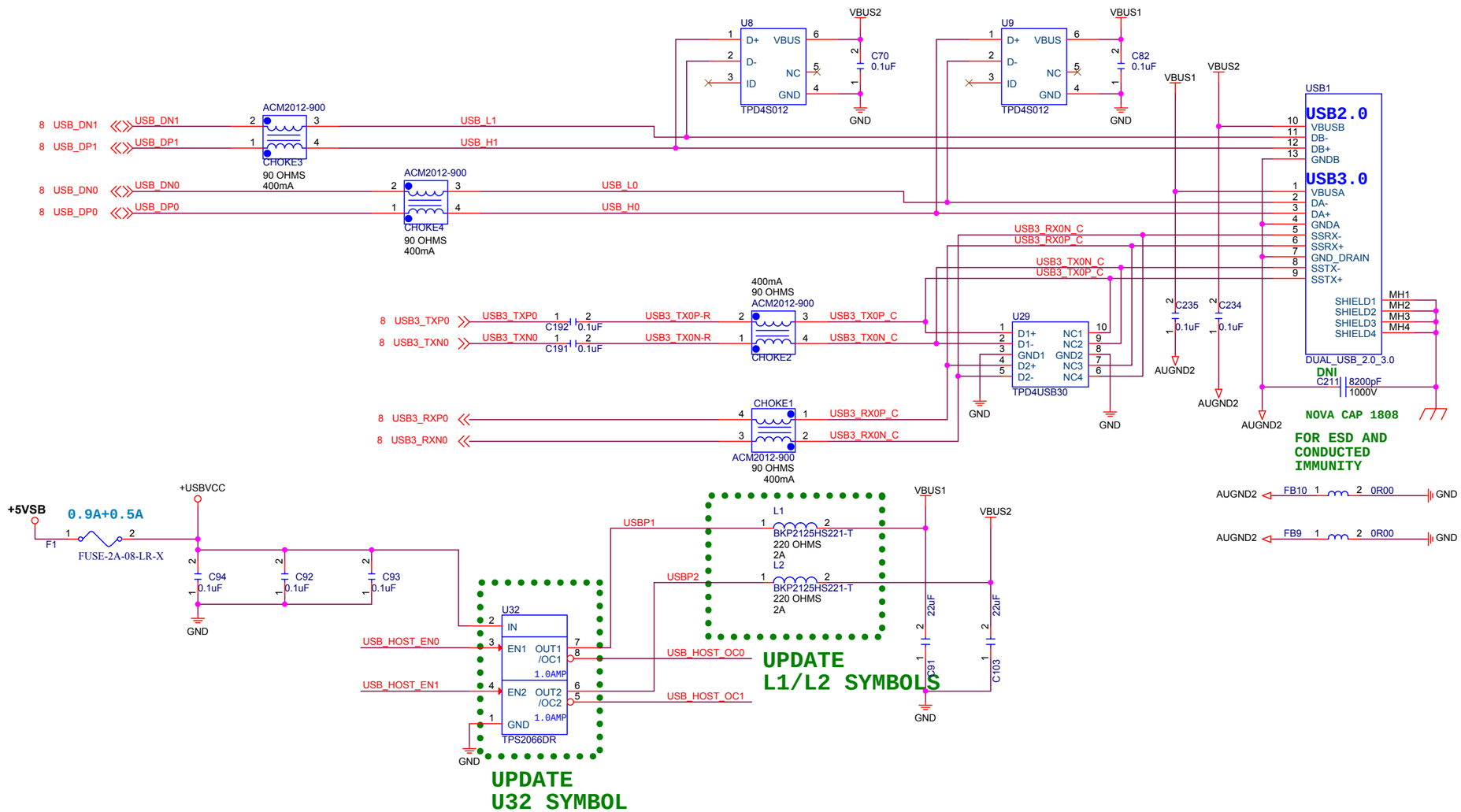

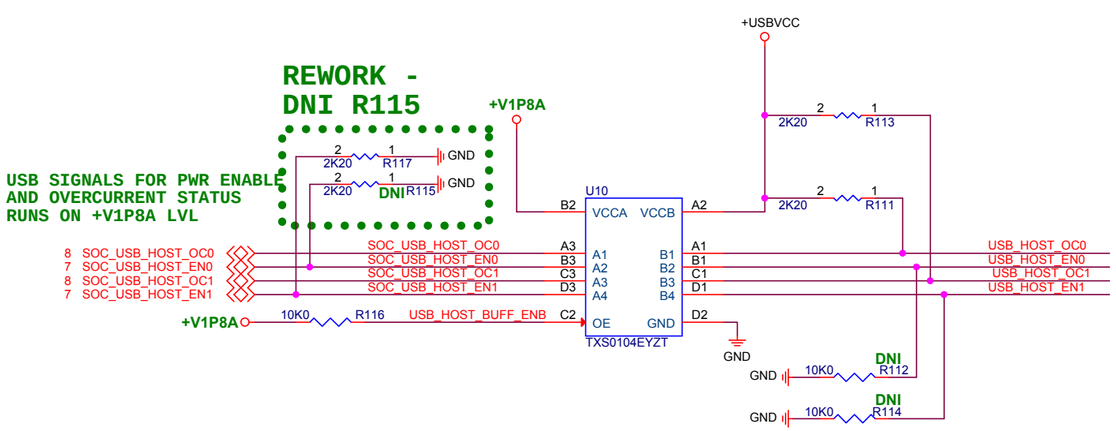

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MINNOWBOARD2 - USB3+USB2

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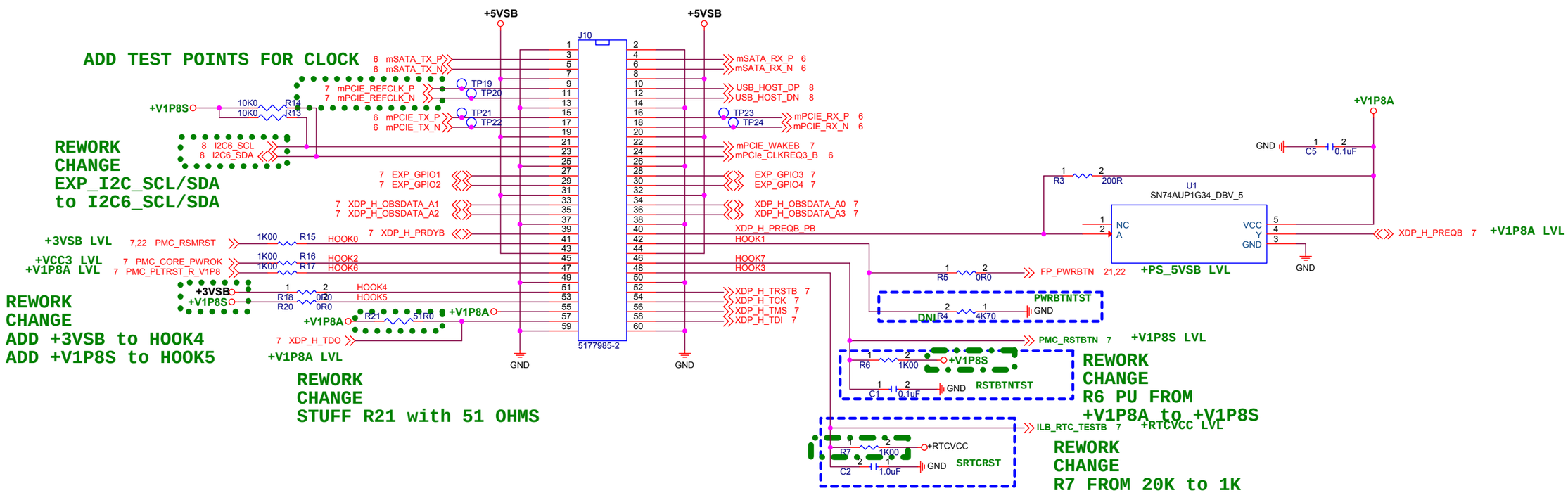
EXPANSION HS CONNECTOR WITH mPCIE, mSATA, I2S AUDIO, GPIO, and XDP I/O



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MINNOWBOARD2 - EXPANSION CONNECTOR I/O

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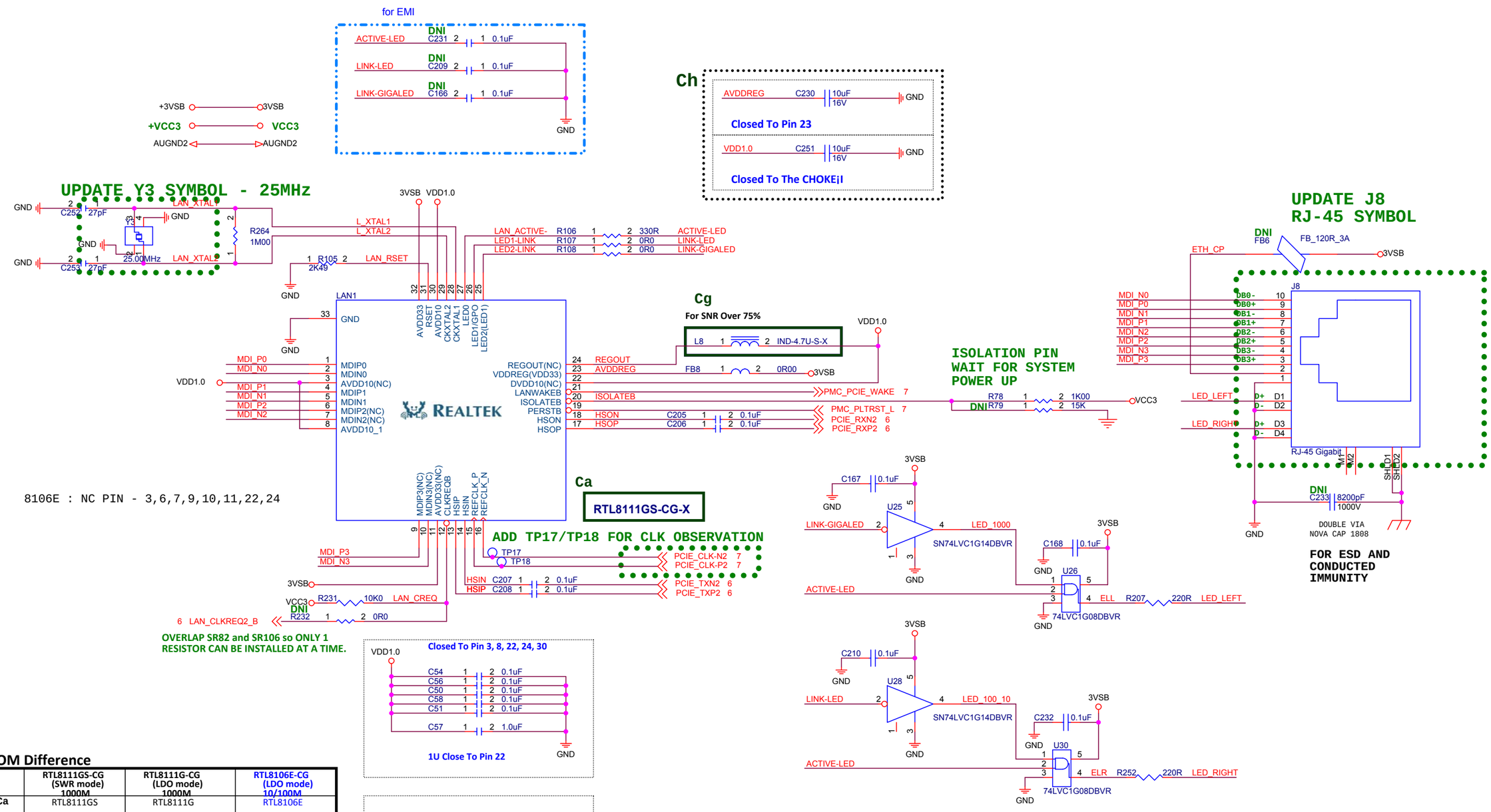

BOM Difference

	RTL8111GS-CG (SWR mode) 1000M	RTL8111G-CG (LDO mode) 1000M	RTL8106E-CG (LDO mode) 10/100M
Ca	RTL8111GS	RTL8111G	RTL8106E
Cb	None	None	None
Cc	USBX2-LAN-1000	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	X	V
Ce	0-04	0-04	.01U-25VX-04
Cf	V	V	X
Cg	L	R	X
Ch	V	X	X

DEFAULT

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MINNOWBOARD2 - LAN RT8111GS-CG

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MINNOWBOARD2 - AUDIO-ALC282

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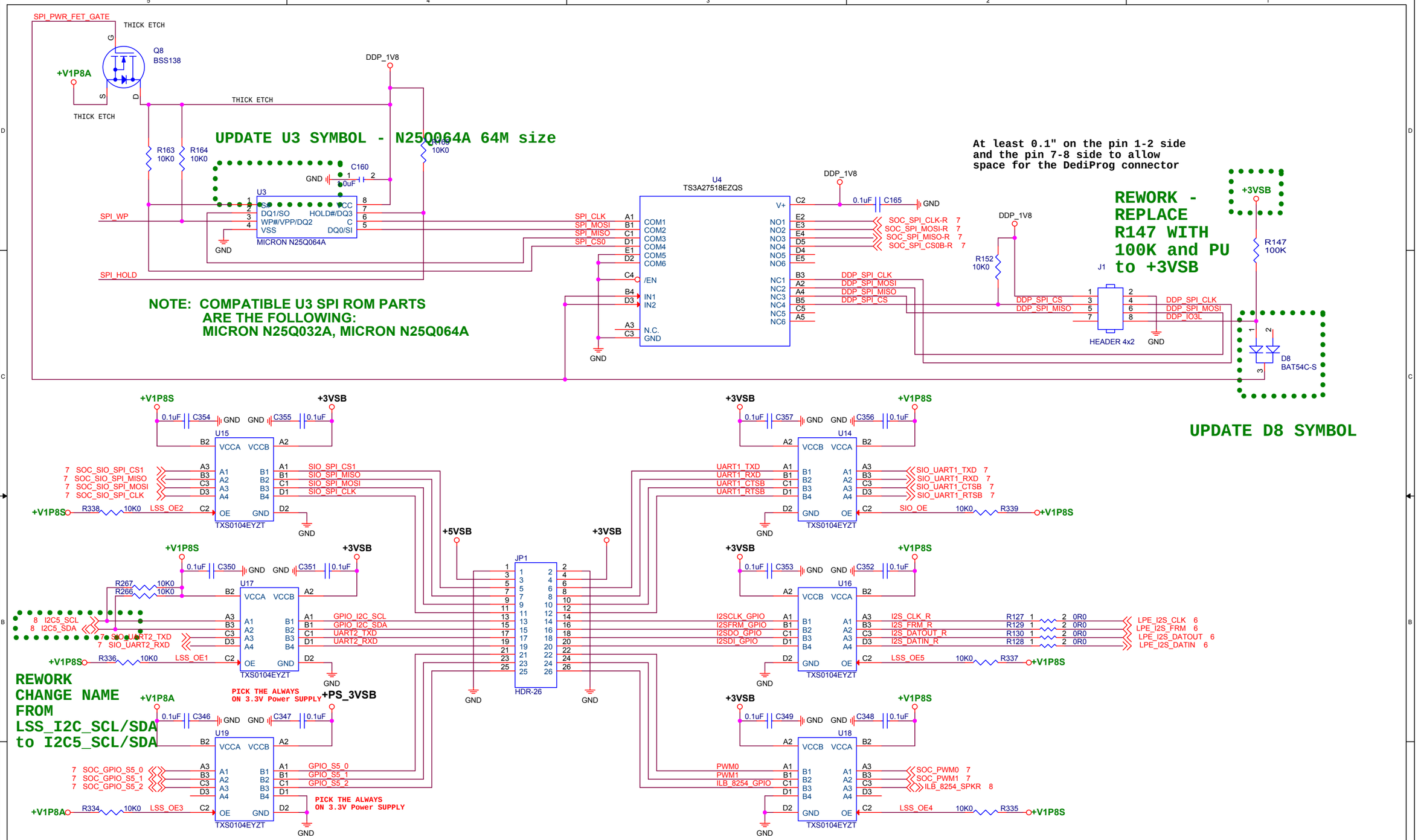

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MINNOWBOARD2 - SPI PROM/LSS HEADER

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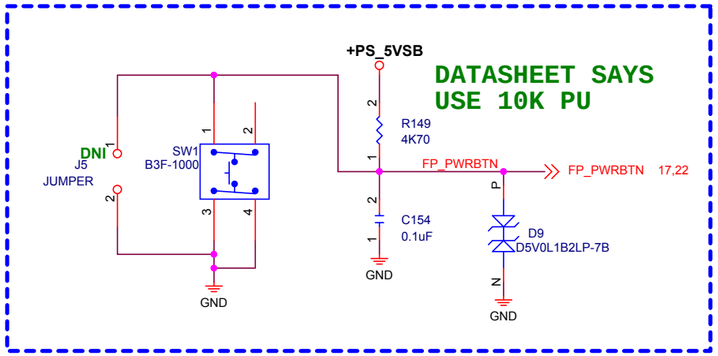
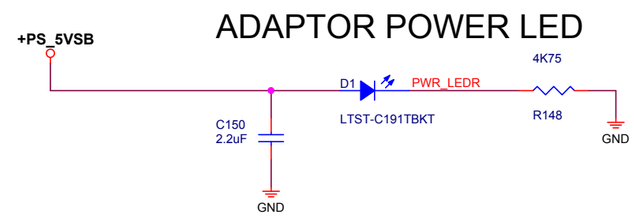
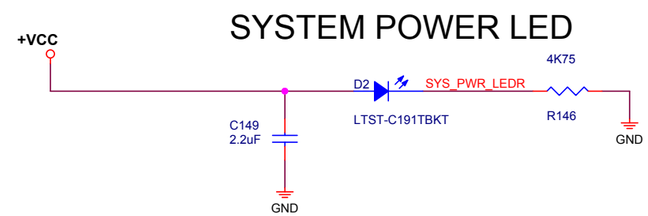
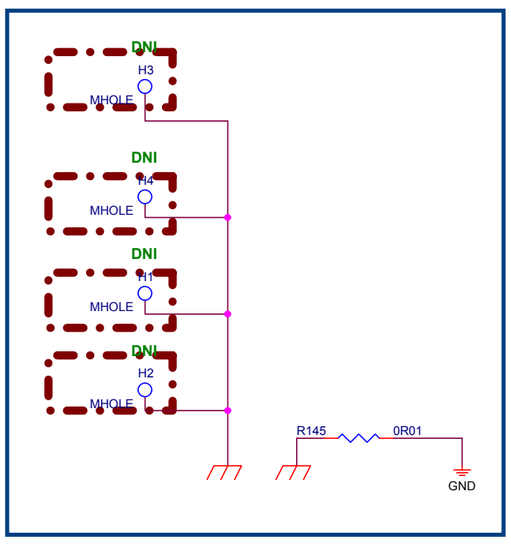






CHANGE MTG HOLES TO
6/32

BOARD HOLES - 4 TOTAL - 1 in EACH CORNER



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MINNOWBOARD2 - PWR BTN / LED / HOLES

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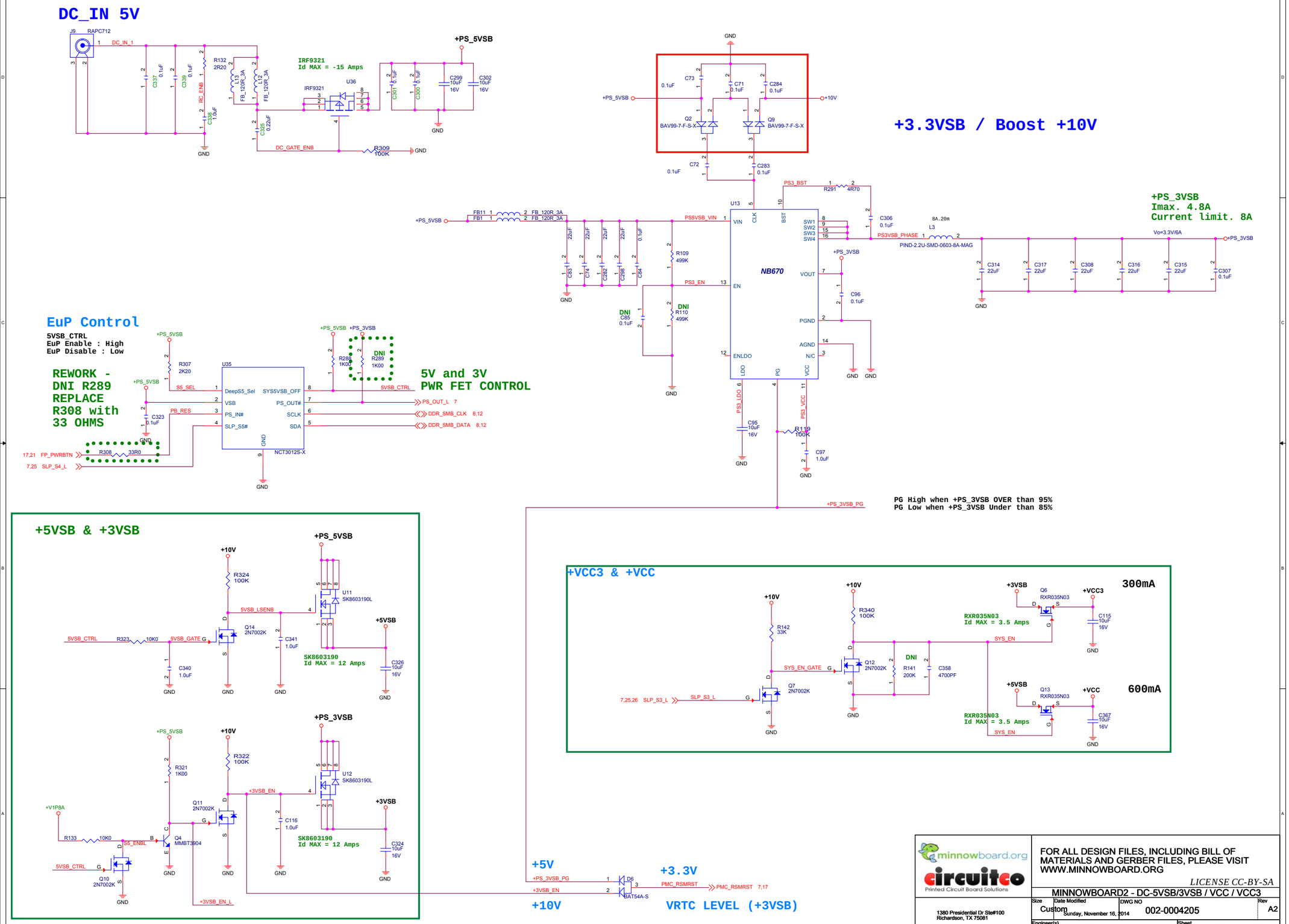

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MINNOWBOARD2 - DC-5VSB/3VSB / VCC / VCC3

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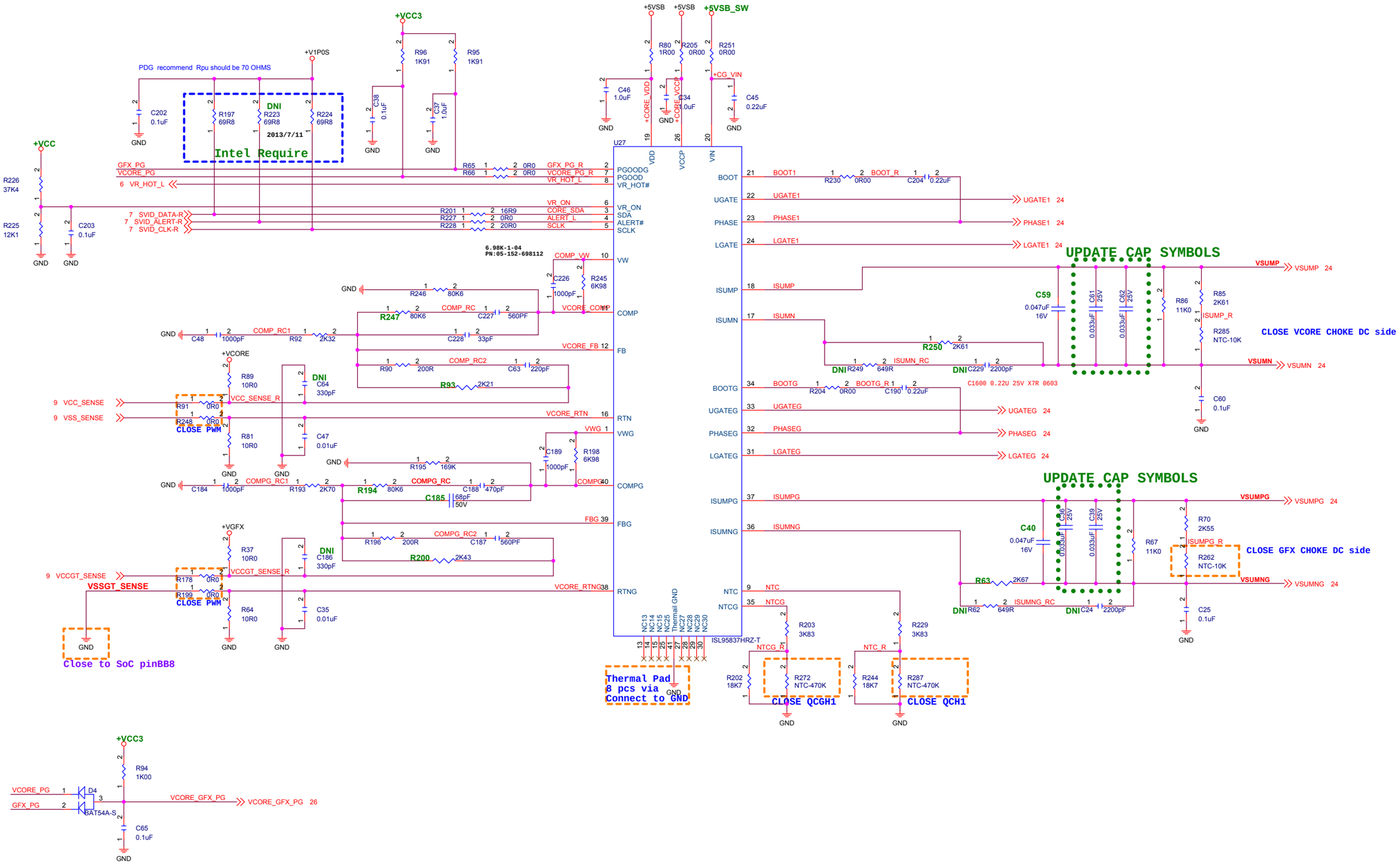

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MINNOWBOARD2 - +5VSB/+3VSB

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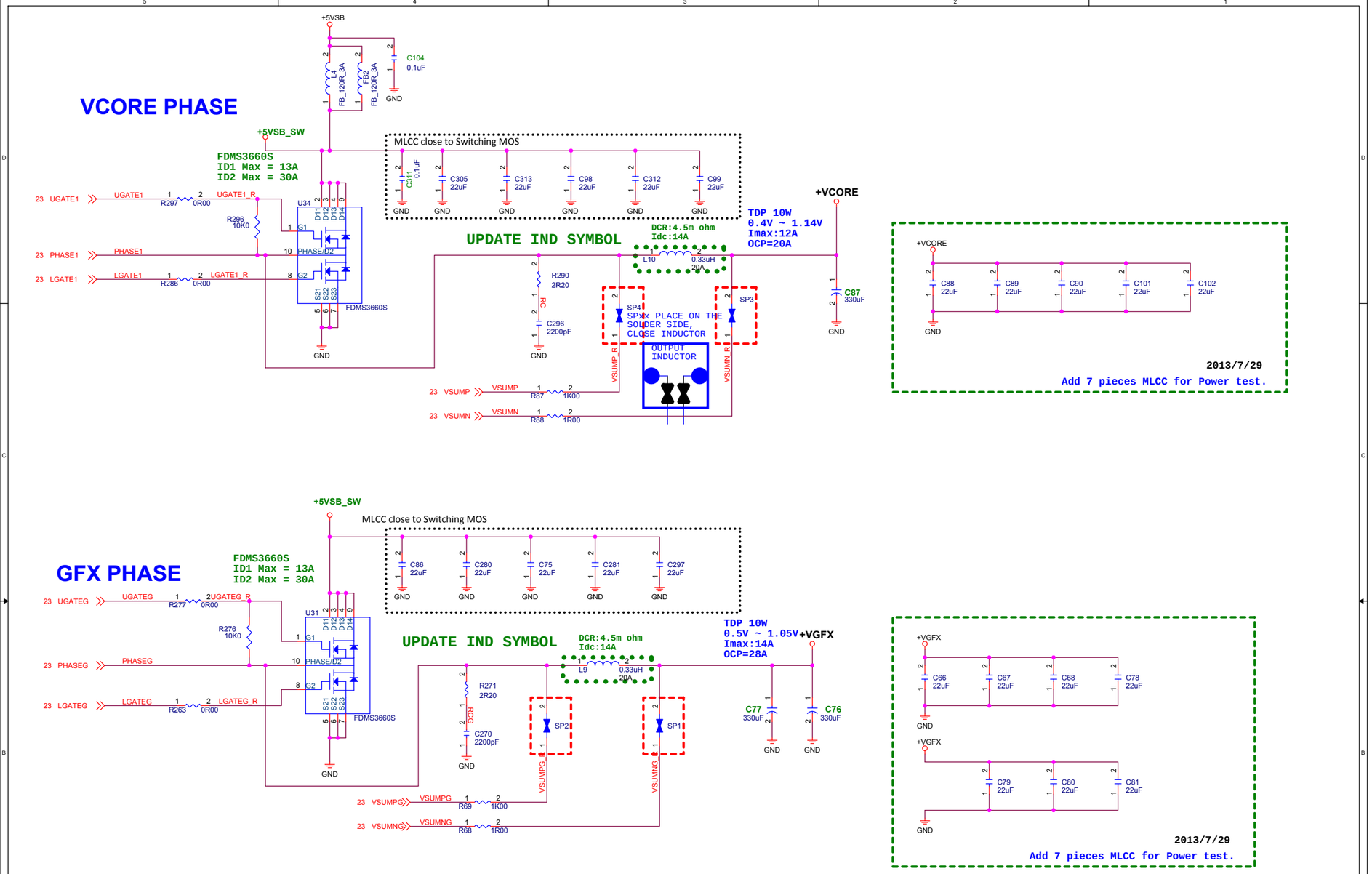

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MINNOWBOARD2 - DC/DC VCORE/GFX MOS

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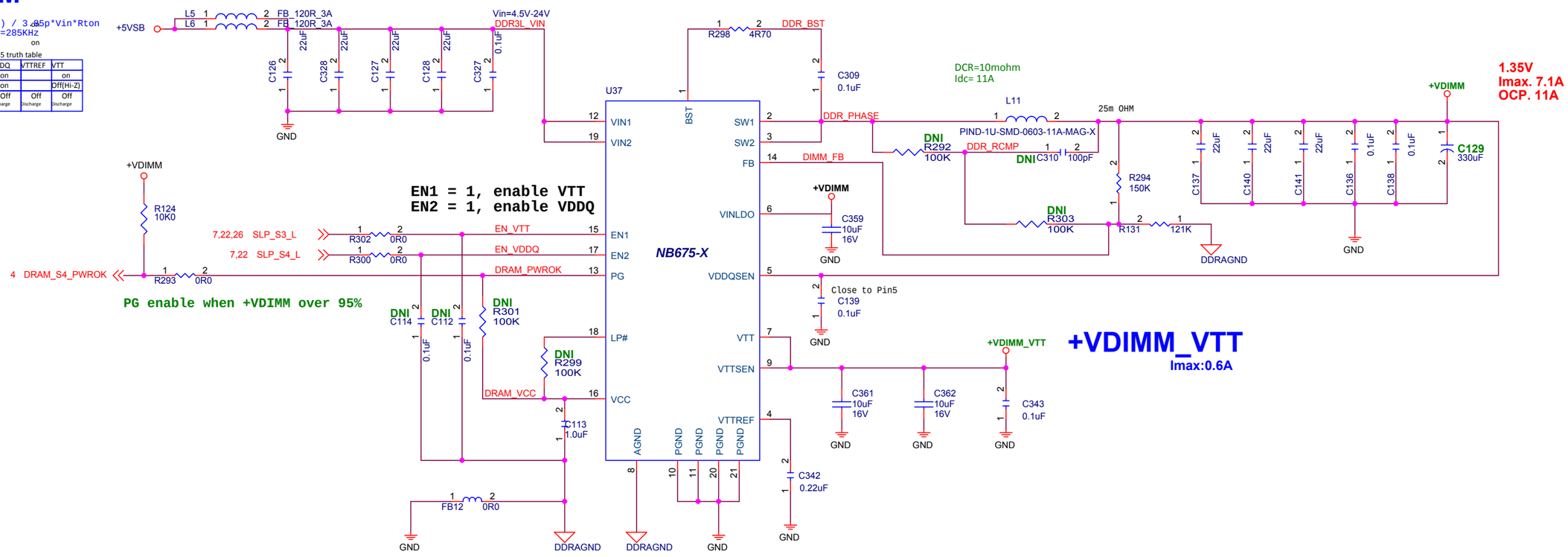
VDIMM

F= (Vin - 0.5) / 3.45p*Vin*Rton
Rton=806K , F=285KHz

RT8207M S3 and S5 truth table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	on		on
S3	Lo	Hi	on		Off(Hi-Z)
S4/S5	Lo	Lo	Off Discharge	Off Discharge	Off Discharge



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MINNOWBOARD2 - DC-DIMM/DDR_VTT

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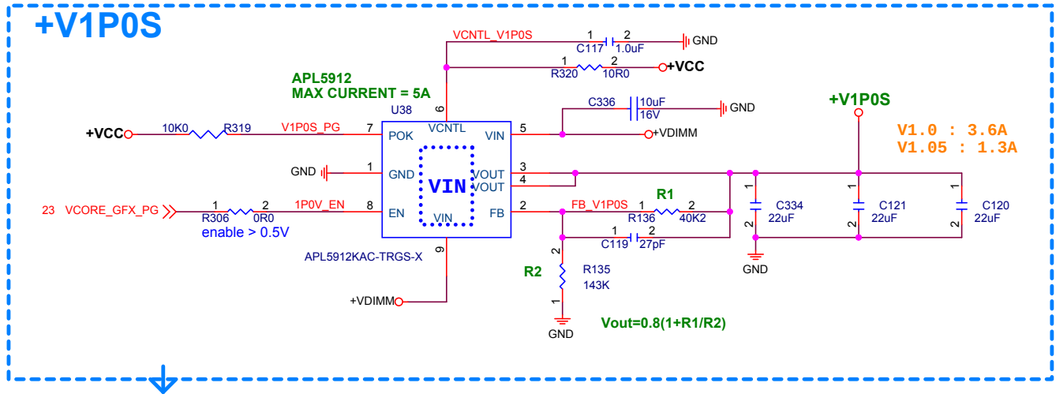

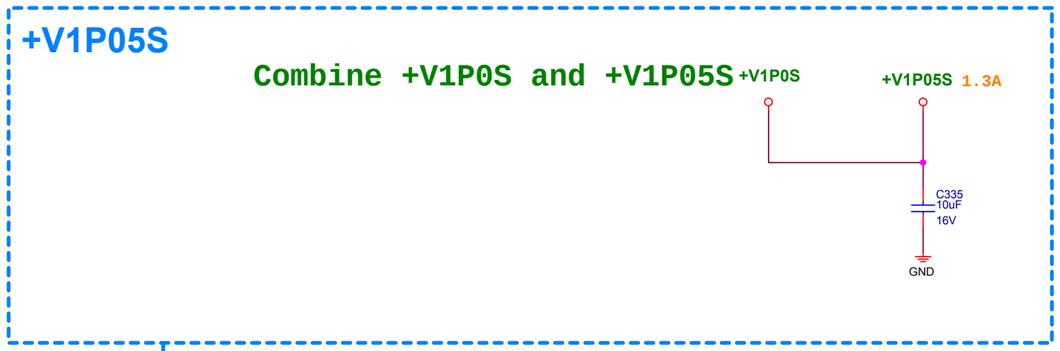

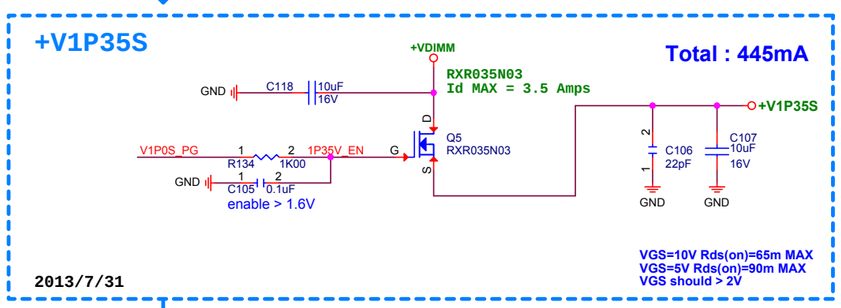

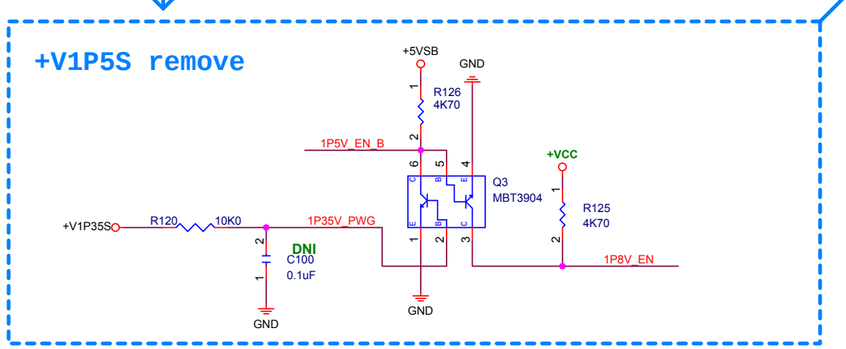

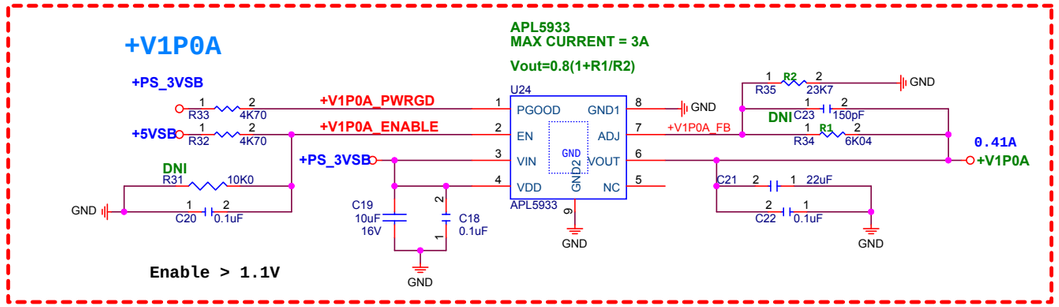

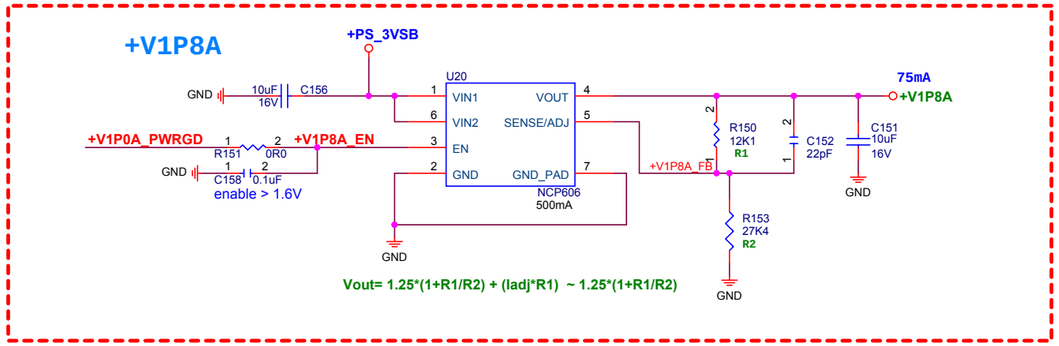

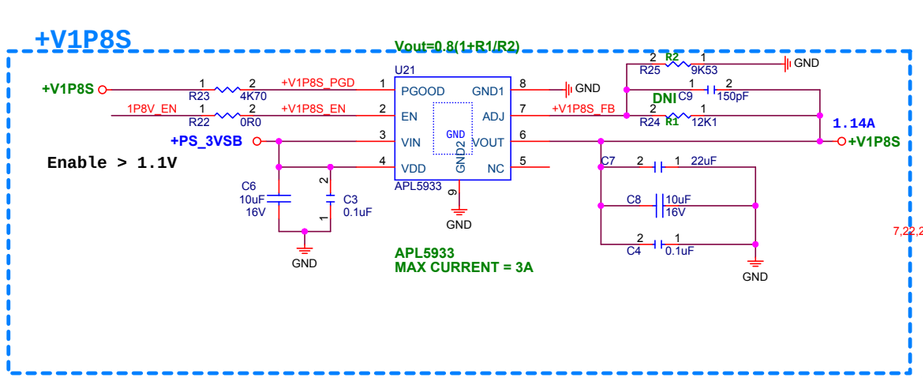

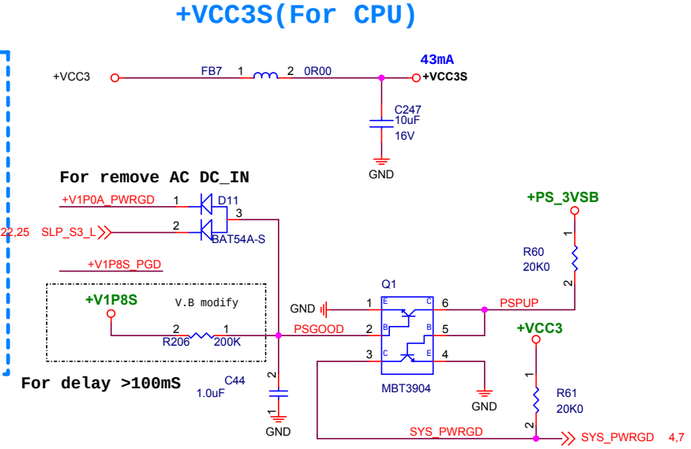

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MINNOWBOARD2 - DC-DC VOLTAGE

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PCH-GPIO function

Pin Name	Power Well	Usage	Boot Set
GPIO_S5[00]	1P8VSB, 20k,H	SOC_GPIO_S5_0 (LSS CONN)	GPO
GPIO_S5[01]	1P8VSB, 20k,H	SOC_GPIO_S5_1 (LSS CONN)	GPO
GPIO_S5[02]	1P8VSB, 20k,H	SOC_GPIO_S5_2 (LSS CONN)	GPO
GPIO_S5[03]	1P8VSB, 20k,H	mPCIE_WAKEB	GPI
GPIO_S5[04]	1P8VSB, 20k,L	OPEN	GPO
GPIO_S5[05]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[06]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[07]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[8]	1P8VSB, 20k,H	HDMI_DC_DC ENABLE	GPO
GPIO_S5[9]	1P8VSB, 20k,H	HDMI LD SWITCH ENABLE	GPO
GPIO_S5[10]	1P8VSB, 20k,H	TXE UNLOCK control	GPO
GPIO_S0_SC[022]	1P8V, 20k,H	OPEN	GPO
GPIO_S0_SC[023]	1P8V, 20k,H	XDP_H_OBSDATA_A0	GPO
GPIO_S0_SC[024]	1P8V, 20k,H	XDP_H_OBSDATA_A1	GPO
GPIO_S0_SC[025]	1P8V, 20k,H	XDP_H_OBSDATA_A2	GPO
GPIO_S0_SC[026]	1P8V, 20k,H	XDP_H_OBSDATA_A3	GPO
GPIO_S0_SC[027]	1P8V, 20k,H	EXPANSION_BUS GPIO1	GPO
GPIO_S0_SC[028]	1P8V, 20k,H	EXPANSION_BUS GPIO2	GPO
GPIO_S0_SC[029]	1P8V, 20k,H	EXPANSION_BUS GPIO3	GPO
GPIO_S0_SC[030]	1P8V, 20k,H	EXPANSION_BUS GPIO4	GPO
GPIO_S0_SC[058]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[059]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[060]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[057]	1P8V, 20k,H	Debug Port UART3 TXD	UART
GPIO_S0_SC[061]	1P8V, 20k,H	Debug Port UART3 RXD	UART

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is unchanged 1 = Top address bit is inverted
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

Interrupt mapping

Function	INT# port	PCIe*1 port	Device
LAN	INTC#	port 2	RTL8111GS-CG

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MINNOWBOARD2 - GPIO/HW MAPPING

Size	Date Modified	DWG NO	Rev
Custom	Sunday, November 16, 2014	002-0004205	A2

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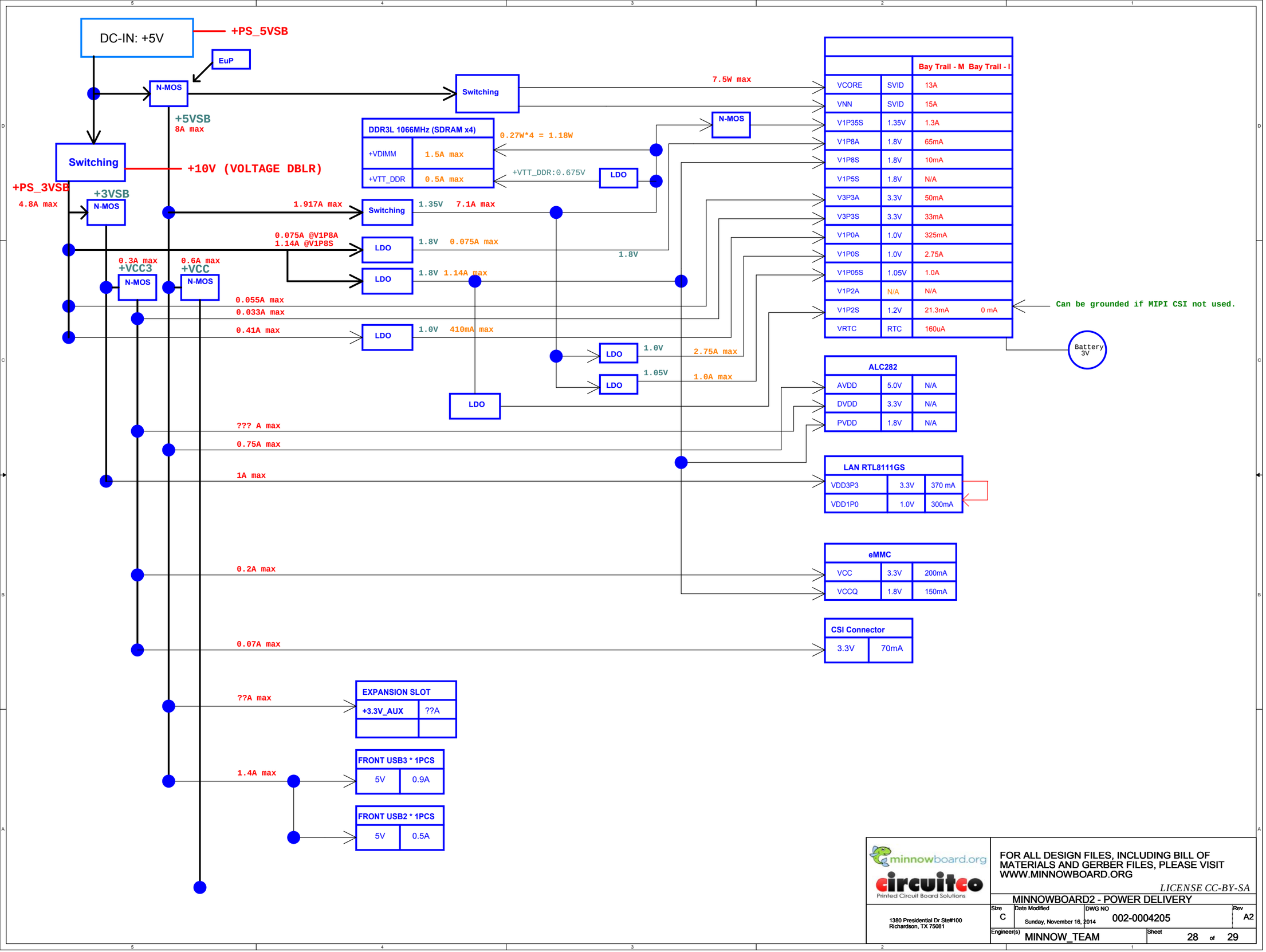

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MINNOWBOARD2 - POWER DELIVERY

Size	Date Modified	DWG NO	Rev
C	Sunday, November 16, 2014	002-0004205	A2

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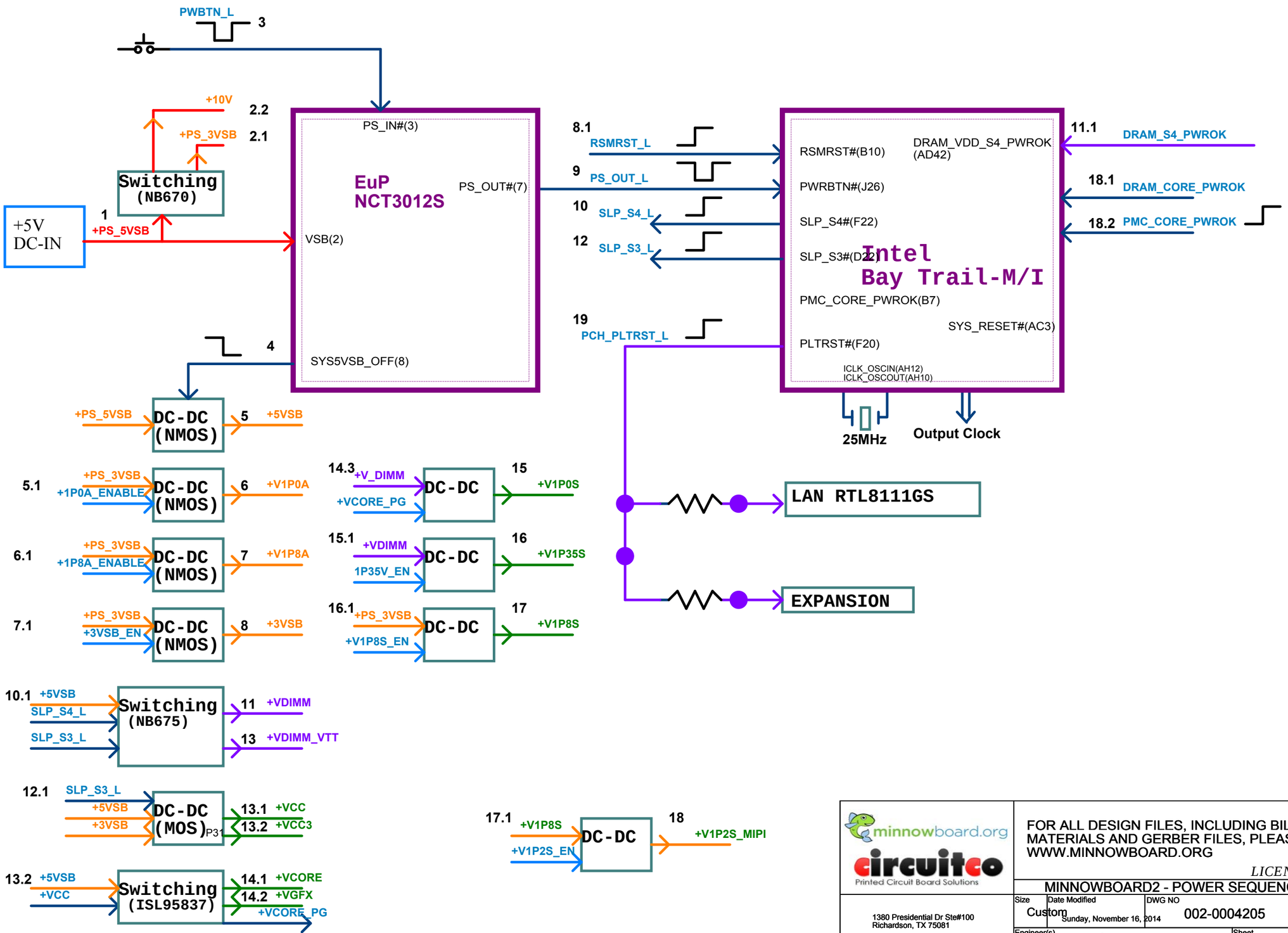
PWR Sequence & RST Diagram



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MINNOWBOARD2 - POWER SEQUENCE

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